TAMAGAWA SEIKI CO.,LTD.

Smartcoder®

AU6803
AU6804

USERS MANUAL

DRAFT 20120209

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Safety Precautions

Before use smartcoder, please carefully read the specification and this manual for proper use. Incorrect usage do not operate normally, may damage the equipment that is connected to this product or this product.
Retain this manual, and please re-read when in doubt.

■Notes

Smartcoder (AU6803, AU6804) is an integrated circuit (i.e electronic device) with a high grade quality level, but the predictable failure rate is not zero. Also there are some possibility to do unplanned work cause of noise, static electricity, wiring error, etc. The user is advised, therefore, that multiple safety means be incorporated in your system or product so as to prevent any consequential troubles resulting from the failure of our smartcoder (AU6803, AU6804).

These application samples which listed in this manual are reference examples. If you use these examples, please make sure that you understand your system, equipments, and those functions and safety.

And the content written in this manual might be changed as needed. For the latest content, please contact your sales representative.

■Product Warranty

(1) Warranty Period

The warranty period for Smartcoder (AU6803, AU6804) is one year after shipping. Failed products within this warranty period will be replaced with new one.

(2) Coverage

Even if within the warranty period, we will not take responsibility for the products which show quality degradation caused by deviant usage against this document or specification like below.

- In case of usage of unguaranteed condition/environment/handling nonlisted in this manual or specification.
- In case of Remodeling/Repair which is not done by Tamagawa-seiki.
- In case of misusing this product.
- In case of unforeseen matters which can not expect at technology level of shipping age.

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1. Introduction

1.1 Product Overview

Smartcoder (AU6803：For automotive、AU6804：For general use※) is an R/D (Resolver to Digital) conversion IC used with a brushless Resolver (BRX) such as Singlsyn, Smartsyn, etc. It converts the electrical information (analog signal) corresponding to a mechanical rotational angle of the Resolver to the corresponding digital data and output it.

It adopted the newly developed "Twin-PLL" R/D conversion method. And it was developed as simple usage, low cost, and having high quality, while maintaining high reliability that the Resolver (Synchro) system has had conventionally. It provides you wide range applications for angle detection.

※ The difference between AU6803 and AU6804 means excuting burn-in process or not. AU6803 applied burn-in process. The functions and characteristics are same.

1.2 Product Features

■Real time output

Max tracking rate : 240,000min^{-1} (External CLK:10MHz～12MHz Operation)、
Max angular acceleration : 1,000,000rad/s^2.

■All-in-one design

Eliminates phase adjustment of exciting signal (allowable phase angle ：±45° while exciting signal 1 period is 360°). Implemented a Oscillator and a excitation amplifier (current control type) help to reduce system cost.

■Small・Light weight

7×7mm (Pin pitch: 0.5mm、48pin-LQFP、weight: 0.3g)。 Achieve half package area against conventional product (AU6802N1).

■Enhance error detection function

Followings are implemented. Abnormal Resolver Signal; Breaking of Resolver Signal Line; Abnormal R/D conversion; Abnormal High temperature inside IC.

■Implemented BIST(Built-In Self Test) function

R/D conversion function and breaking detection of signal line can be tested themselves.

■Rich output form

Binary-code Parallel 12bit Bus compatible、Positive logic＋ A,B,Z ＋ Serial I/F.

■DC+5V Single Power Supply

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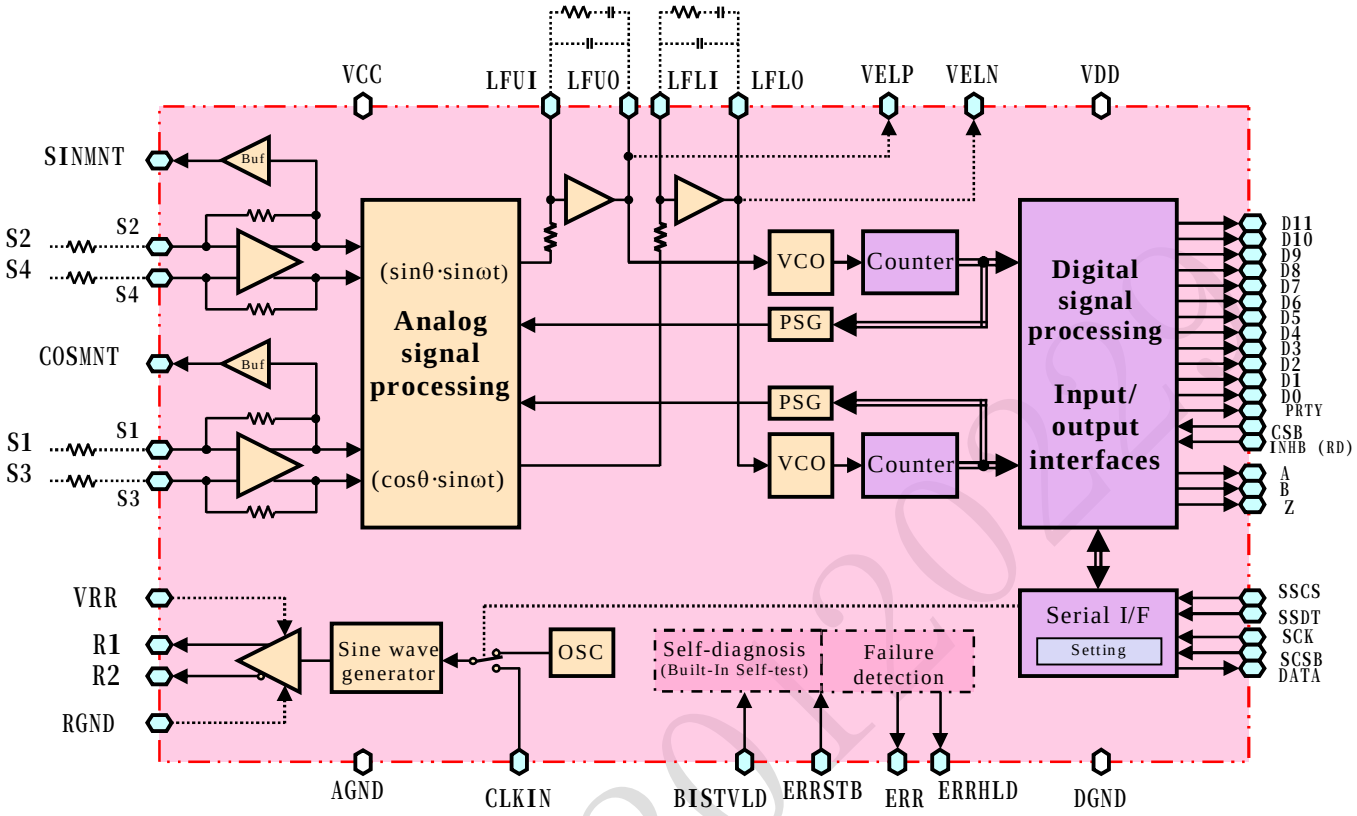
1.3 Block Diagram



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1.4 Spec Overview

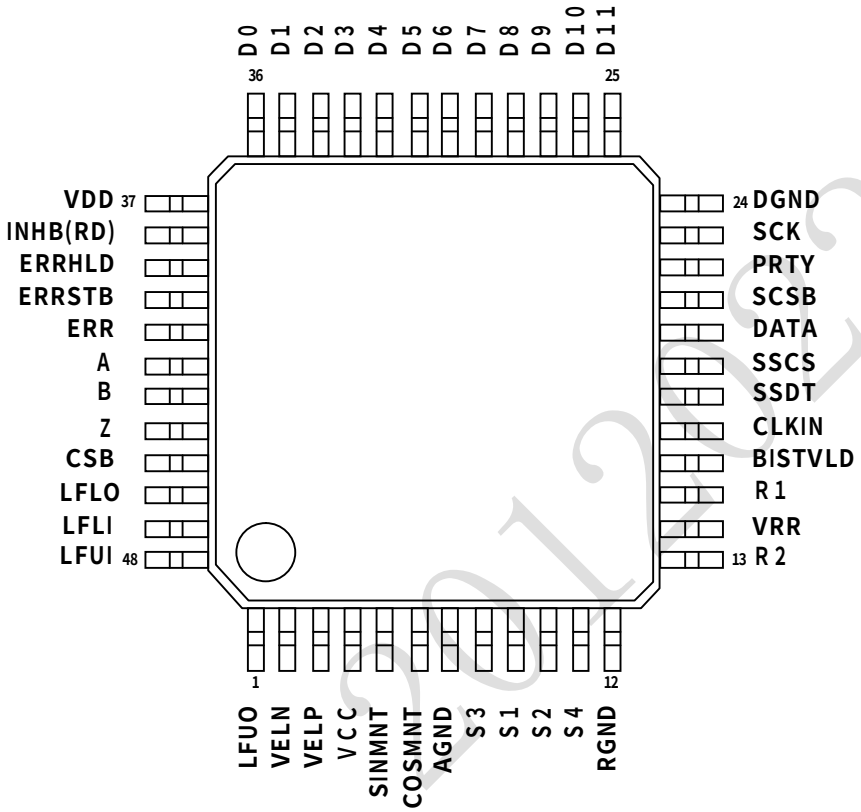
Output form	Binary code parallel 12bit bus compatible, Positive logic ＋ A, B, Z ＋ Serial I/F	
Resolution	4,096 (2^{12})	
Conversion accuracy (Static)	±4 LSB	
Settling time (Step input 180 ° in electric angle)	1.5 ms typ.	
Max. tracking rate	240,000 min^{-1} (10MHz＜External CLK≦12MHz Operating)	180,000 min^{-1} (Internal CLK or 8MHz＜External CLK≦10MHz operating)
Max. angular acceleration	1,000,000 rad / s^2	
Response (As output response delay in electric angle)	±0.2 ° Max./10,000 min^{-1}	
Encorder emulation output(A,B)	1,024 C/T	
Resolver excitation amplifier (current control type)	9.5mArms、10kHz typ.	
Fault detection function	・Abnormal resolver signal ・Breaking of resolver signal line ・Abnormal R/D conversion ・Abnormal high temperature inside IC	
BIST function (BIST：Built-In Self Test)	・BIST of R/D conversion (Test for R/D conversion) ・BIST of failure detection (Test for broken wire)	
Power source	DC 5V±10% 60mA max.	
Operating temperature	-40 ～ +125°C	
Storage temperature	-65 ～ +150°C	
Humidity	90% RH max. (No condensation)	
Mass	0.3g max.	

1.5 Related Documents

(1) SPC007898Y00 Twin-PLL type smartcoder AU6803 Specifications
(2) SPC008948Y00 AU6804 specification (Japanese version)

2. Pin List (Name and Functions)

2.1 Pin Assignment



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2.2 Pin Description

Pin No	Symbol	Class	Description	Remarks (Reference chapter #)
1	LFUO	A／O	External filter connection terminal. Connect recommended electorical components to LFUI terminal.	(4.2.3)
2	VELN	A／O	Differential analog velocity outputs. The voltage corresponding to the velocity output between VELP-VELN.	(4.2.4)
3	VELP	A／O		
4	VCC	——	Analog power pin. Connect to +5V.	(4.4)
5	SINMNT	A／O	Resolver signal(SIN) monitor output. Input gain should be adjusted to be approximately 2Vp-p for this pin.	(4.2.2)
6	COSMNT	A／O	Resolver signal(COS) monitor output. Input gain should be adjusted to be approximately 2Vp-p for this pin.	
7	AGND	——	Analog ground pin. Connect to 0V.	(4.4)
8	S3	A／I	Resolver signal (S3) input pin. This signal enters through the gain setting resistor of resolver signal input circuit.	(4.2.2)
9	S1	A／I	Resolver signal (S1) input pin. This signal enters through the gain setting resistor of resolver signal input circuit.	
10	S2	A／I	Resolver signal (S2) input pin. This signal enters through the gain setting resistor of resolver signal input circuit.	
11	S4	A／I	Resolver signal (S4) input pin. This signal enters through the gain setting resistor of resolver signal input circuit.	
12	RGND	——	Exciting amplifier ground pin. Connect to 0V.	(4.4)
13	R2	A／O	Exciting output (R2) pin. Sinusoidal waveform current 9.5mArms(typ) which can excite resolver directly output between R1-R2.	(4.2.1)
14	VRR	——	Exciting amplifier power pin. Connect to +5V.	(4.4)
15	R1	A／O	Exciting output (R1) pin. Sinusoidal waveform current 9.5mArms(typ) which can excite resolver directly output between R1-R2.	(4.2.1)
16	BISTVLD	D／I	BIST function control pin. BIST function can run when BISTVLD is L level and serial setting resistor set for BIST operation code. BIST control / Excutable / Not excution BISTVLD / L / H	(7)
17	CLKIN	D／I	Clock input pin for external clock mode. Input clock frequency should be in a range of 10MHz±20%.	(4.3.3 (2))
18	SSDT	D／I	Serial setting data input pin. While SSCS is "L", the input SSDT data is synchronized to SCK and set to pre-setting register. The data load to control register at SSCS ascending timing, then new system setting will be made.	(4.3.1 (2))
19	SSCS	D／I	Chip Select pin for serial input setting function. This signal control SSDT data reception and renewal system setting at ascending timing. If you do not use serial input function, please connect to VDD. SSDT Chip Select / Accepted / Not accepted SSCS / L / H	
20	DATA	D/O (BUS)	Serial data output pin. When SCSB input falls down, serial output data transmit with synchronization to the SCK.	(4.3.2 (2))
21	SCSB	D／I	Chip Select pin for serial output function. This signal control DATA pin output and latch transmitting data when SCSB input falls down. DATA pin out / Data output / Hi Impedance SCSB / L / H	
22	PRTY	D/O (BUS)	Even parity signal pin for output data (D0～D11). "H" lebel number of D0～D11,PRTY pins must be even.	
23	SCK	D／I	Serial Clock input pin. Use for serial input setting function and serial output function. Max frequency is 5MHz.	(4.3.1 (2) , 4.3.2 (2))
24	DGND	——	Digital ground pin. Connect to 0V.	(4.4)

(Note) "Class" means as follo.

* A／I : Analog input
* A／O : Analog output
* D／I : Digital input
* D／O (BUS) : Digital output (3-state output)

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<table>
<tr><th>Pin No</th><th>Symbol</th><th>Class</th><th colspan="2">Description</th><th>Remarks
(Reference chapter #)</th></tr>
<tr><td rowspan="2">25</td><td rowspan="2">D11</td><td rowspan="2">D/O (BUS)</td><td>Absolute output mode</td><td>Pulse output mode</td><td rowspan="13">(4.3.2(1))</td></tr>
<tr><td>φ1 (MSB)</td><td>ERRCD3</td></tr>
<tr><td>26</td><td>D10</td><td>D/O (BUS)</td><td>φ2</td><td>ERRCD2</td></tr>
<tr><td>27</td><td>D 9</td><td>D/O (BUS)</td><td>φ3</td><td>ERRCD1</td></tr>
<tr><td>28</td><td>D 8</td><td>D/O (BUS)</td><td>φ4</td><td>ERRHLD</td></tr>
<tr><td>29</td><td>D 7</td><td>D/O (BUS)</td><td>φ5</td><td>ERR</td></tr>
<tr><td>30</td><td>D 6</td><td>D/O (BUS)</td><td>φ6</td><td>—</td></tr>
<tr><td>31</td><td>D 5</td><td>D/O (BUS)</td><td>φ7</td><td>W</td></tr>
<tr><td>32</td><td>D 4</td><td>D/O (BUS)</td><td>φ8</td><td>V</td></tr>
<tr><td>33</td><td>D 3</td><td>D/O (BUS)</td><td>φ9</td><td>U</td></tr>
<tr><td>34</td><td>D 2</td><td>D/O (BUS)</td><td>φ10</td><td>Z</td></tr>
<tr><td>35</td><td>D 1</td><td>D/O (BUS)</td><td>φ11</td><td>B</td></tr>
<tr><td>36</td><td>D 0</td><td>D/O (BUS)</td><td>φ12 (LSB)</td><td>A</td></tr>
<tr><td>37</td><td>VDD</td><td>——</td><td colspan="2">Digital power pin. Connect to +5V.</td><td>(4.4)</td></tr>
<tr><td>38</td><td>INHB(RD)</td><td>D／I</td><td colspan="2">Inhibit (Read) pin. This signal switchs through/hold for below corresponding pins.
■Absolute output mode：φ1～φ12, PRTY
■Pulse output mode：U, V, W, ERR, ERRHLD, ERRCD1～3
<table><tr><th>Target output pin status</th><th>Through</th><th>Hold</th></tr><tr><td>INHB(RD)</td><td>H</td><td>L</td></tr></table></td><td>(4.3.2)</td></tr>
<tr><td>39</td><td>ERRHLD</td><td>D／O (I)</td><td colspan="2">ERR (Hold) pin. Once an abnormal condition is detected, this signal change to “H” and keep this level until error reset.
This pin also serves as the default output mode setting for D0～D11. It is excuted by sensing the voltage level at power-up as an input pin, which has a pull-up resistor(10kΩ) or pull-down resistor(10kΩ).
<table><tr><th>D0～D11 default setting</th><th>Absolute out mode</th><th>Pulse out mode</th></tr><tr><td>ERRHLD pin treatment</td><td>10kΩ pull-up</td><td>10kΩ pull-down</td></tr></table></td><td>(8,
4.3.1 (1))</td></tr>
<tr><td>40</td><td>ERRSTB</td><td>D／I</td><td colspan="2">Error reset pin. This signal reset ERRHLD and ERRCD1～3.
<table><tr><th>ERRHLD,ERRCD1～3 status</th><th>Hold</th><th>Clear (reset)</th></tr><tr><td>ERRSTB</td><td>H</td><td>L</td></tr></table></td><td>(8.6)</td></tr>
<tr><td>41</td><td>ERR</td><td>D／O (I)</td><td colspan="2">ERR output pin. While the error is detected, output “H” level.
This pin also serves as the default mode setting for operation clock. It is excuted by sensing the voltage level at power-up as an input pin, which has a pull-up resistor(10kΩ) or pull-down resistor(10kΩ).
<table><tr><th>Clock default setting</th><th>Internal oscillator</th><th>External clk input</th></tr><tr><td>ERR pin treatment</td><td>10kΩ pull-up</td><td>10kΩ pull-down</td></tr></table></td><td>(8,
4.3.1 (1))</td></tr>
<tr><td>42</td><td>A</td><td>D／O</td><td colspan="2">Equivalent to an encoder A pulse output pin.</td><td rowspan="2">(4.3.2 (3))</td></tr>
<tr><td>43</td><td>B</td><td>D／O</td><td colspan="2">Equivalent to an encoder B pulse output pin.</td></tr>
<tr><td>44</td><td>Z</td><td>D／O (I)</td><td colspan="2">Equivalent to an encoder Z pulse output pin.
This pin also serves as the default mode setting for excitation mode. It is excuted by sensing the voltage level at power-up as an input pin, which has a pull-up resistor(10kΩ) or pull-down resistor(10kΩ).
<table><tr><th>Excitation mode default setting</th><th>Current excitation</th><th>Voltage excitation</th></tr><tr><td>Z pin treatment</td><td>10kΩ pull-up</td><td>10kΩ pull-down</td></tr></table></td><td>(4.3.2 (3) ,
4.3.1 (1))</td></tr>
<tr><td>45</td><td>CSB</td><td>D／I</td><td colspan="2">Chip select(CSB) pin. This signal controls D0～D11,PRTY pins.
<table><tr><th>D0～11,PRTY pin setting</th><th>Data output</th><th>Hi Impedance</th></tr><tr><td>CSB</td><td>L</td><td>H</td></tr></table></td><td>(4.3.2 (1))</td></tr>
<tr><td>46</td><td>LFLO</td><td>A／O</td><td colspan="2">External filter connection terminal.
Connect recommended electorical components to LFLI terminal.</td><td>(4.2.3)</td></tr>
<tr><td>47</td><td>LFLI</td><td>A／I</td><td colspan="2">External filter connection terminal.
Connect recommended electorical components to LFLO terminal.</td><td>(4.2.3)</td></tr>
<tr><td>48</td><td>LFUI</td><td>A／I</td><td colspan="2">External filter connection terminal.
Connect recommended electorical components to LFUO terminal.</td><td>(4.2.3)</td></tr>
</table>

(Note) “Class” means as follow.

* A／I : Analog input
* A／O : Analog output
* D／I : Digital input
* D／O : Digital output
* D／O (I) : Digital output (With internal pull-up for input)
* D／O (BUS) : Digital output (3-state output)

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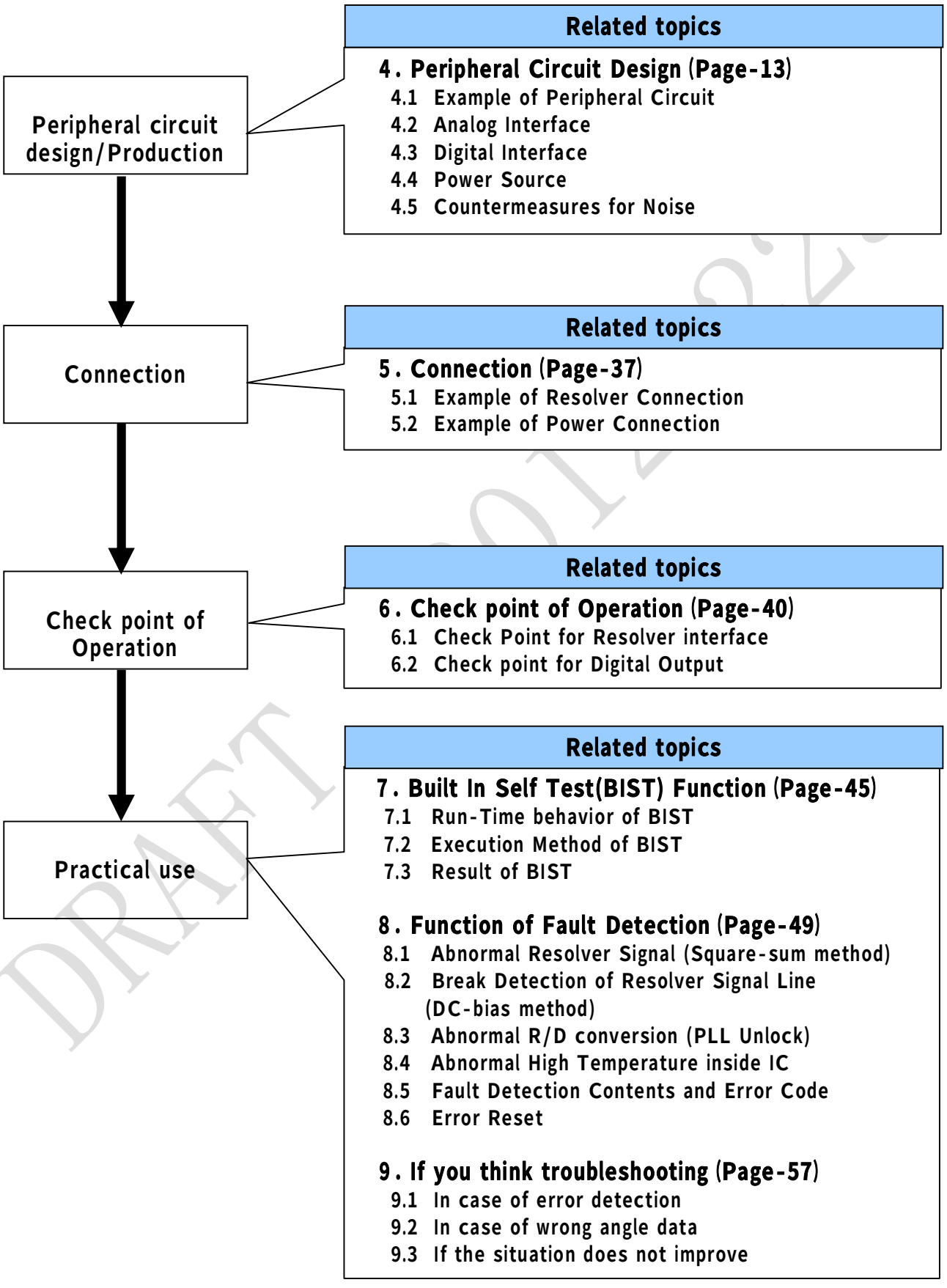
3. Setup Flow



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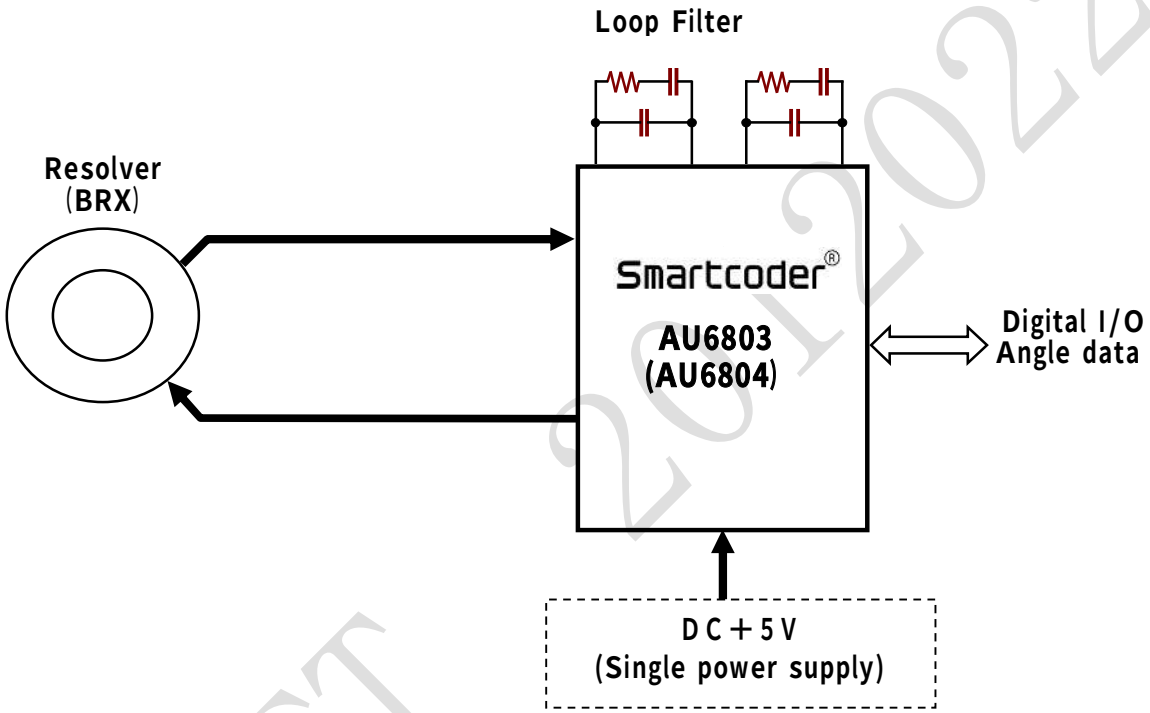
4. Peripheral Circuit Design

AU6803/AU6804 require some peripheral circuit to get digital angle data. In this chapter, we explain the design method and important point for required peripheral circuit design.

4.1 Example of Peripheral Circuit



※ Some applications will require an external clock input and separate excitation amplifier.

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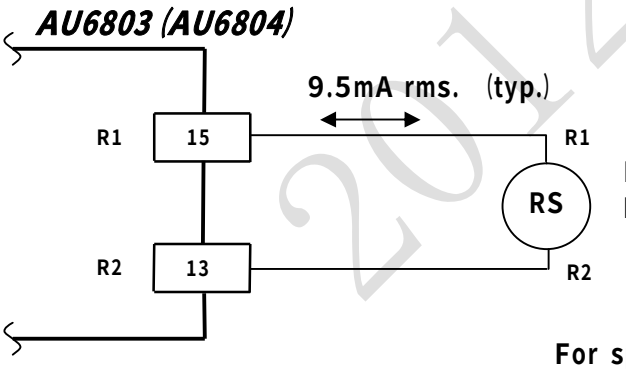
4.2 Analog Interface

※ Examples mentioned in this articles shows only the concept of basic functions. Please note that each application might have their each individual requirement. Therefore the circuit configulation and the decision of constants for practical resistors and the function of protection for input/output circuits, etc. should be designed for each application by customer.

4.2.1 Resolver Excitation Circuit

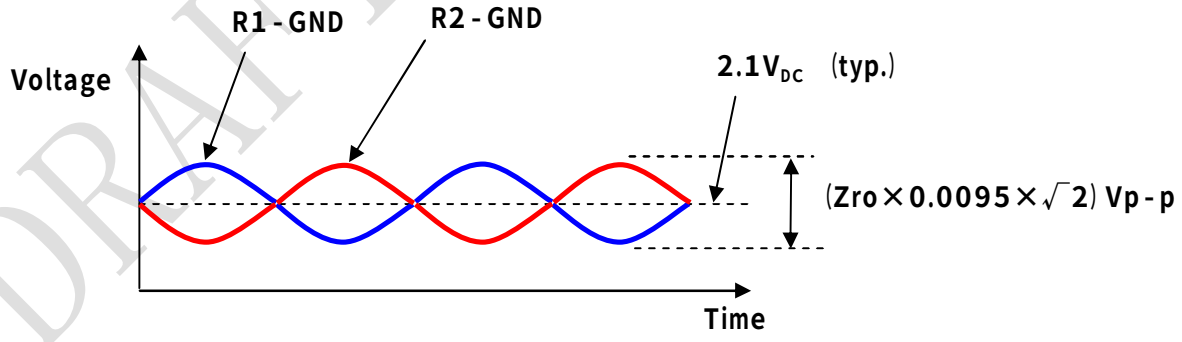
(1) Direct Excitation

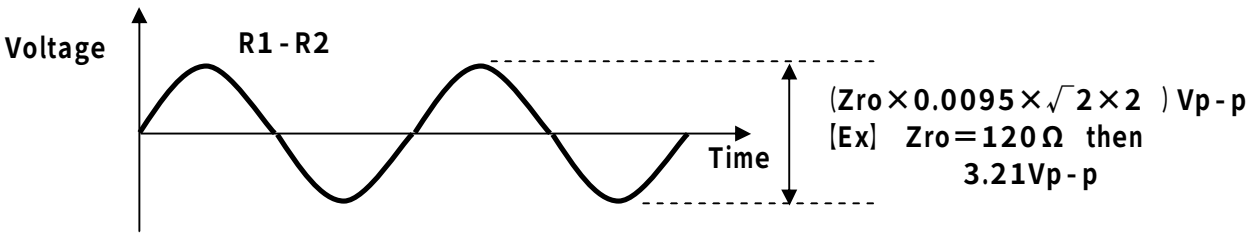
AU6803 (AU6804) has an excitation amplifier in the IC then it is possible to excite resolver directly. It is constant-current amplifier and its current value is 9.5mArms (typ). In case you do not put separate amplifier, it is ideal for cost-sensitive application usage.
Note that the lower the input impedance value shows lower exciting voltage then it need noise considerations. In such case, exciting voltage booster amplifier can be placed separately as shown in the following section.



Resolver
Input Impedance : Zro [Ω]

For specific circuit configuration, please refer to P37.





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(2) Separate excitation amplifier

In case of severe noise environments, exciting voltage booster amplifier can be placed separately. There are 2 type of excitation amplifier circuit, current control type and voltage control type. Show merit/demerit of each method below. Please determine appropriate method for your system considering them.

Excitation Amp.	Merit	Demerit
Current control type	・Prevention of secondary failure(damage of output TR. Etc.) by short circuit between exciting lines. ・Resolver output fluctuations caused temperature change can be suppressed by a constant excitation current.	・Circuit is getting complex, and it might not operate as caliculations. ・Exciting voltage might vary due to resolver input impedance variability.
Voltage control type	・Circuit is simple and it will operate as caliculations. ・Exciting voltage can be constant.	・Possibility to have secondary failure due to overcurrent in case of short circuit between exciting lines. ・Easier to get the resolver output variation due to temperature changes.

Separate power supply (V_{EXT}) is required for the excitation amplifier circuit, in addition to the AU6803 (AU6804) +5V power supply.

Higher resolver exciting voltage caused higher resolver output voltage and it can expect to improve the S/N ratio or noise immunity. That mean it need appropriate DC power supply. For example, exciting voltage 7Vrms (＝20Vp-p ：$7V \times \sqrt{2} \times 2$) require ＋24V for single power source or ±15V for dual power sources.

Resolver operation will be possible at the lower exciting voltage compared to the value described in the specification. So please decide exciting voltage value considering noise immunity and power equipment which can be prepared.

In this chapter, we will show you the example of excitation amplifier circuit (current control type) using AU6803(AU6804) exciting output(R1,R2).

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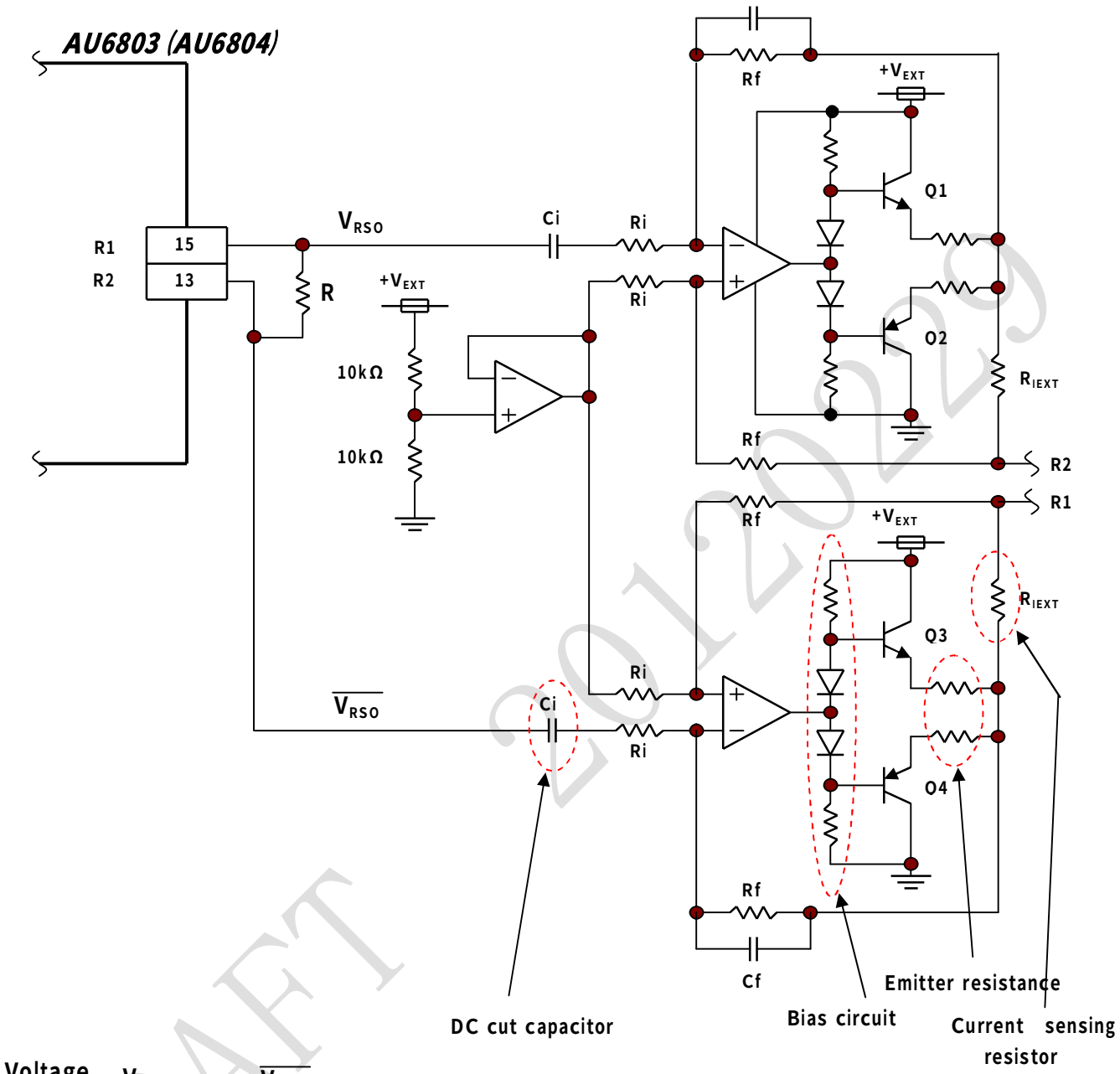
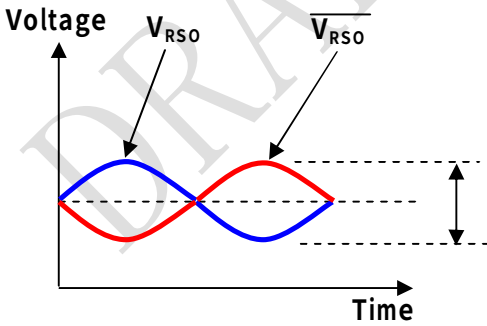
■Example circuit for single power source





[Ex] R=150Ω case

$150 \times 0.0095 \times \sqrt{2}$
$= 2.00 Vp\text{-}p$

In case of V_{EXT} variation is expected by battery power, it must be defined standard operating at minimum voltage.

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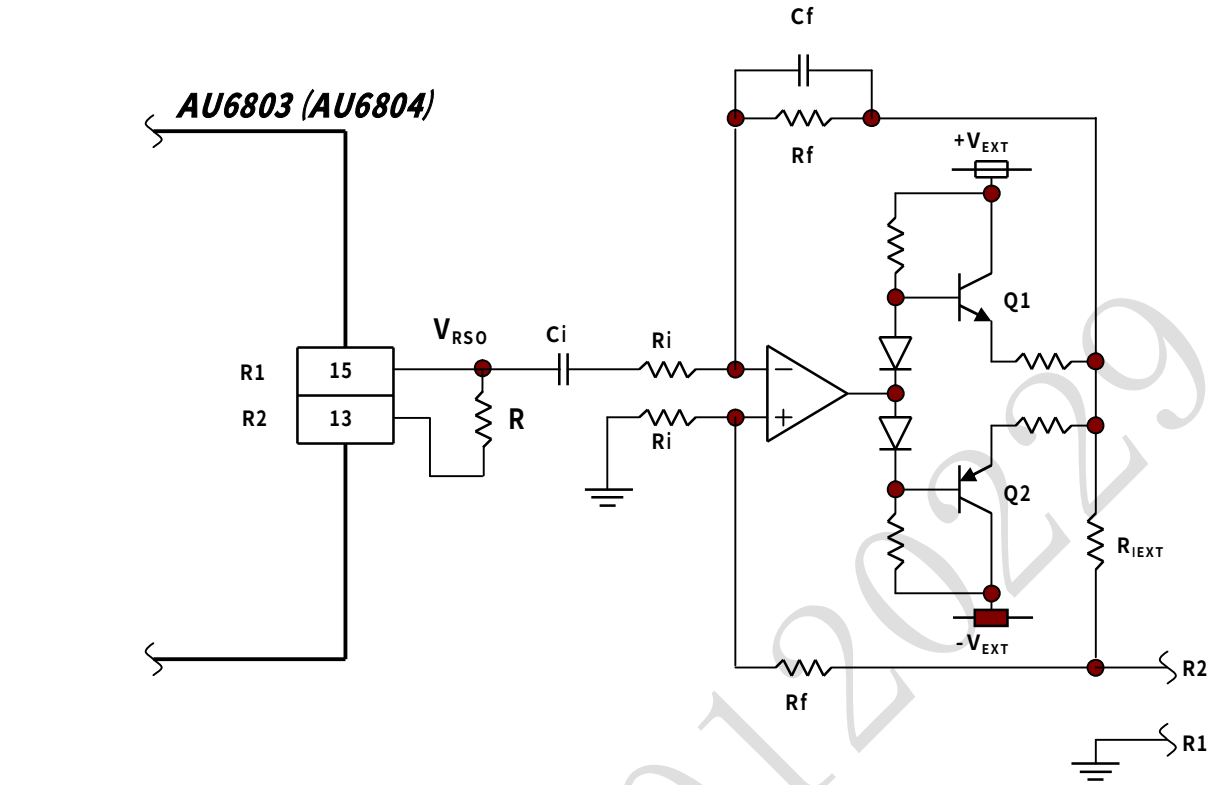
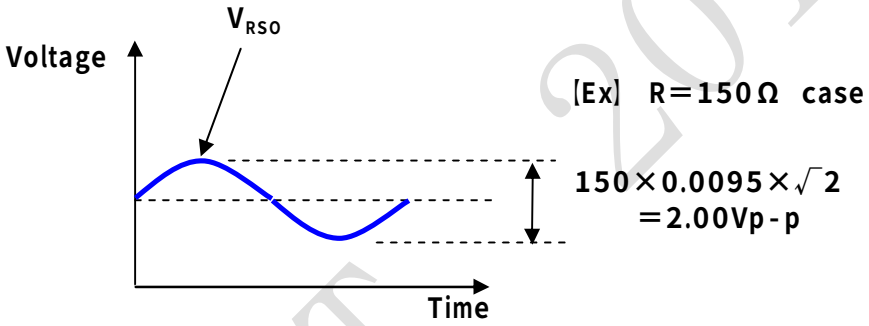
■Example circuit for dual power source





[Ex] R=150Ω case

150×0.0095×√2
=2.00Vp-p

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■Method for Setting constants of separate excitation amplifier (sample)

Refer below for setting constants.

≪Description of symbol≫

$+V_{EXT}$, $-V_{EXT}$: External power supply (For exciting voltage booster amplifier circuit)
I_{REF} : Exciting current of Resolver
R_{IEXT} : Resistor for setting exciting current of Resolver
V_{REF} : Exciting voltage of Resolver
Z_{RO} : Input impedance of Resolver (Specified value)
V_{RSO} : R1 (or R2) pin output voltage

Step① : Calculate the exciting current by setting the exciting voltage based on the voltage of external power supply.

$$V_{REF} = I_{REF} \times Z_{RO}$$

Step② : Calculate the circuit constants based on the exciting current.

$$I_{REF}/2 = (V_{RSO} \times Rf) / (R_{IEXT} \times Ri) \quad \cdots\cdots \text{For single power source}$$

$$I_{REF} = (V_{RSO} \times Rf) / (R_{IEXT} \times Ri) \quad \cdots\cdots \text{For dual power source}$$

< Setting condition>

- $R_{IEXT} \leqq (Z_{RO} / 10)$ [Ω]
- $Rf \geqq 50k\Omega$, $Ci \times Ri \geqq 5 \times 10^{-4}$ [s] , $Cf \times Rf \leqq 5 \times 10^{-6}$ [s]
- The power supply for an operational amplifier should be the same as that for the transistor buffer.

※This calculation method is based on DC circuit concept.
Resolver is a AC circuit and that input impedance (= R(RESISTANCE) +jX(CONDUCTOR)) cause voltage phase shift and current phase shift. Also there are some impacts at parallel connection of Rf and Cf. Then it might not get exact exciting voltage value as calculated.
In such a case, please adjust each constant by yourself. (Voltage can be adjusted by Ri value)
And it is effective to make pre-validation using circuit simulation like SPICE.

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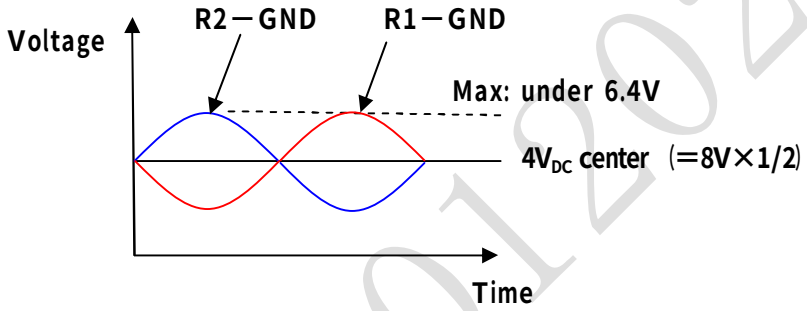
[Example]

V_{EXT}＝Battery 12V (8V～16V fluctuation), Excitation frequency＝10KHz,
Resolver Spec [Input impedance＝76Ω (R-part:18Ω＋L-part:1.18mH)]
Let's excite this resolver with current type amplifier described in P16.

V_{EXT} define as 8V(use minimum fluctuation).
Saturation voltage of OP-AMP assume as x0.8 supply. → 8V×0.8＝6.4V

Regarding R1-GND and R2-GND,
Set amplitude center as $4V_{DC}$ (＝8V×1/2).
Set amplitude as 4Vp-p.
Then target amplitude is set as "R1-R2＝8Vp-p".



According to the formula of P18,

Resolver excitation current (I_{REF}) ＝0.11Ap-p (＝8Vp-p/76Ω)

R_{IEXT}＝4.7Ω ＜ Resolver input impedance (76Ω) /10
Rf＝100kΩ
Then,

$$I_{REF}=\frac{V_{RSO}\times Rf}{R_{IEXT}\times Ri} \quad \cdots\cdots \text{For single power source}$$

$$Ri=\frac{V_{RSO}\times Rf}{R_{IEXT}\times I_{REF}\times 1/2}=\frac{2Vp-p\times 100k}{4.7\times 0.11\times 1/2}$$

＝774kΩ <----> (Please adjust at actual circuit.)

Example of circuit simulation,
Resolver input impedance ＝18Ω＋1.18mH
Cf ＝100p
Emitter resistance ＝4.7Ω
Bias resistance＝1kΩ
Then around Ri ＝ 460k Ω . (8Vp-p between R1-R2)

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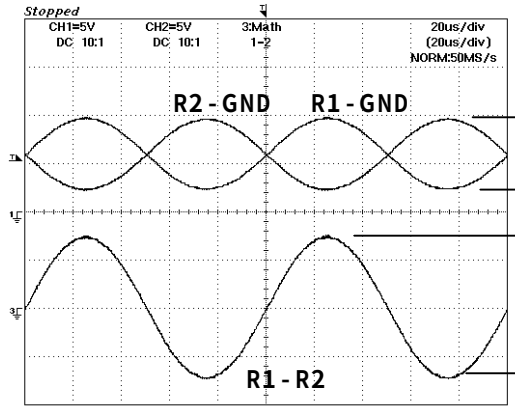
[Single power source V_{EXT}=12V waveform sample]

—Normal operation case—



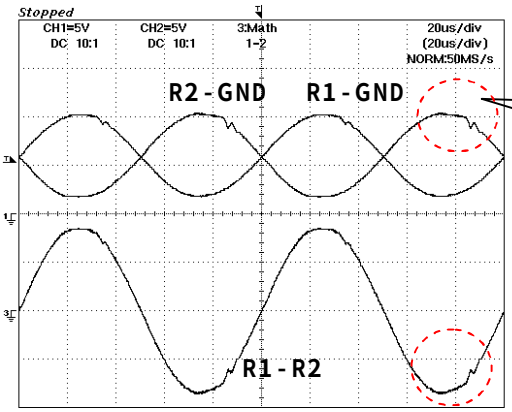
7Vp-p

6V center (=1/2·V_{EXT})

14Vp-p

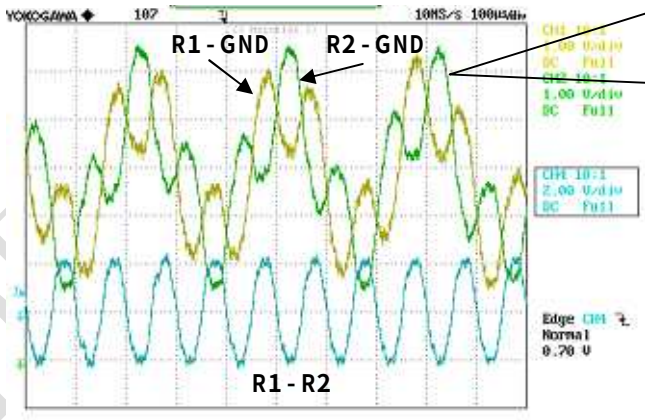
0V center

—Trouble(distortion) case—

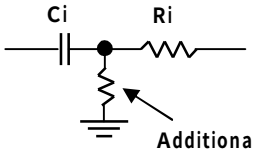


The wrong constant selection cause wider amplitude, and waveform distortion will be occurred by OP-AMP or Tr saturation voltage, etc.
Need to avoid distortion.

Rail to Rail OP-AMP type (saturation voltage is close to supply voltage) can set wider active output voltage without distortion generation.



It might happen to have R1-GND/R2-GND oscilation due to OP-AMP characteristic.
If this kind of wave is observed, DC cut Capacitor (Ci) might cause unstability of DC current. Then insersion of resistor between Ci output and GND will be effective to stabilize it.



Additional resistor
(around 100kΩ)

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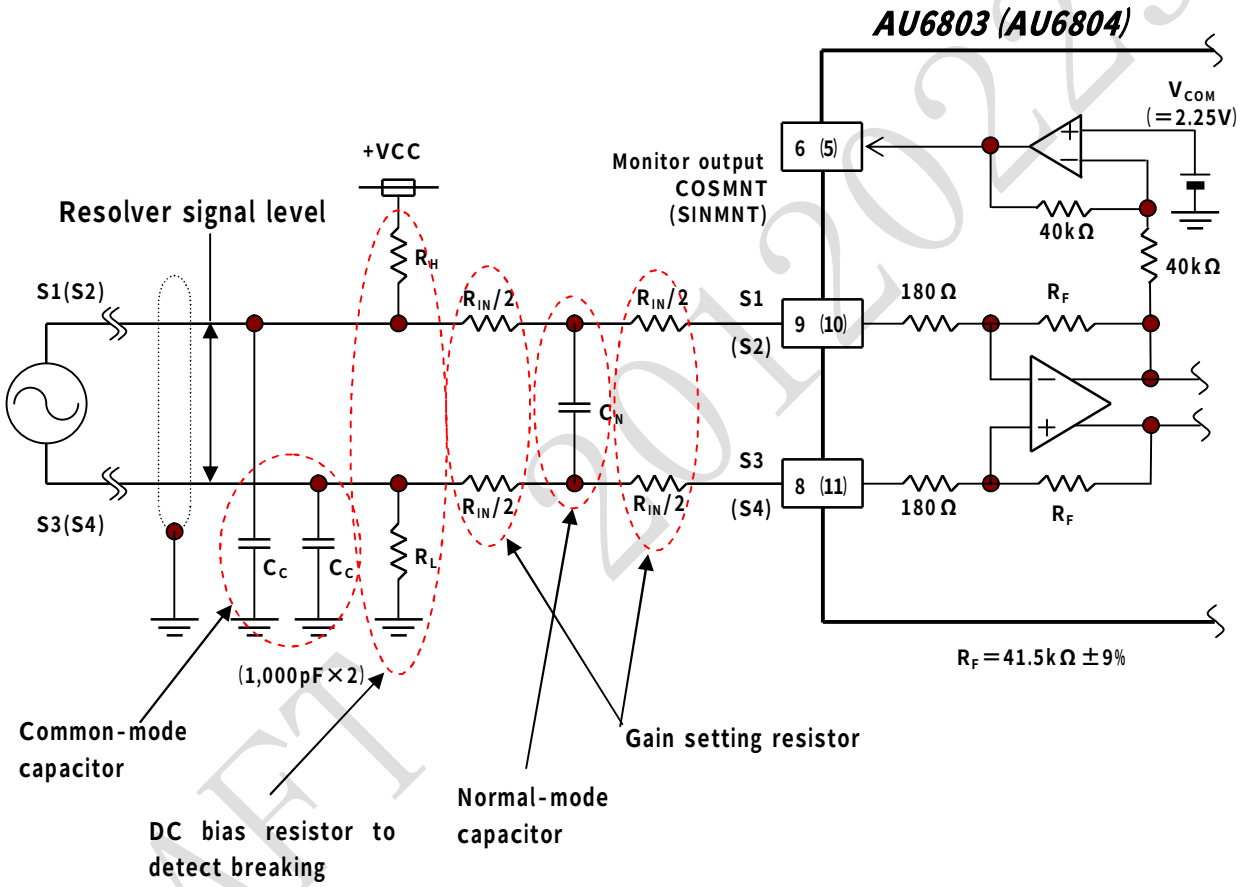
4.2.2 Resolver Signal Input Circuit

R/D conversion of AU6803 (AU6804) will be done with monitor output (SINMNT, COSMNT). While voltage level of resolver signal is different with each application, it need to set appropriate monitor signal level with gain adjustment of resolver input signal to fit R/D conversion effectively. Also it need to have external DC bias resistor activating the function which detect any breaking of Resolver signal lines (S1~S4) mounted in AU6803 (AU6804).

In this chapter, show you example of resolver signal input circuit.

■Example of resolver signal input circuit



(1) Gain setting resistor

The relationship between input resolver signal amplitude and monitor amplitude shows below.

$$\text{Monitor amplitude [Vp-p]} = \text{Resolver signal amplitude [Vp-p]} \times (1/2) \times \frac{R_F}{R_{IN}}$$

Gain setting resistor (R_{IN}) is defined as monitor MAX amplitude 2Vp-p .

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[Example]
Resolver spec (Exciting voltage: AC7Vrms, transformer ratio: 0.286),
Use it as exciting voltage 10Vp-p, monitor output max amplitude assumed 2Vp-p.

Resolver output max＝2.86Vp-p （＝10Vp-p×0.286） then,

$$2.0\ \text{Vp-p} = 2.86\ \text{Vp-p} \times (1/2) \times \frac{41.5\text{k}\Omega}{R_{IN}} \qquad \therefore R_{IN} = 30\text{k}\Omega$$

Note, assumed R_{IN} ≧2kΩ. In case of R_{IN} is close to 2kΩ,

$$\text{Monitor amplitude [Vp-p]} = \text{Resolver signal amplitude [Vp-p]} \times (1/2) \times \frac{R_F}{R_{IN} + 180\Omega}$$

Like above, please consider input resistance (=180Ω) .

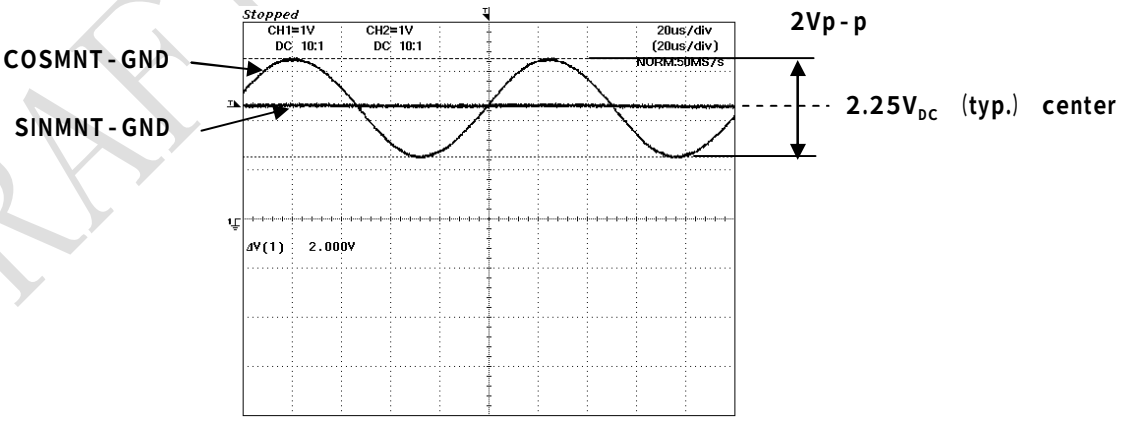
※If potential difference between SINMNT and COSMNT generate by the deviation of R_{IN}, it will caused error source. Please select appropriate resistor grade according to your system tolerance.

[Example] In case of there is a ＋Δ COSMNT against SINMNT,

$$\text{Error} = -\frac{1}{2} \cdot \Delta \cdot \text{SIN2}\theta \quad [\text{rad}]$$

(Voltage difference 1% case: Δ＝0.01 Then Error max.＝±0.29 ° （＝±0.01/2 [rad])

Example of monitor waveform （At 0 °)



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(2) DC bias resistor to detect breaking (R_H, R_L)

When the signal line come down, monitor output level must be exceeded the threshold value and it need to set appropriate resistance value.

(1) R_H $\{(4.5-V_{COM}) / (12.5\times10^{-6})\} - R_{IN}$

(2) R_L $\{V_{COM} / (12.5\times10^{-6})\} - R_{IN}$ While $V_{COM}=2.25[V]$

Resistor value is determined in the range of 80~100% of the caliculated value.

In general, $R_H, R_L = (180k\Omega - R_{IN}) \times (0.8\sim1.0)$

Without this DC bias resistor, fault detection depend on its angle (Could be detect at somewhere in rotation).

(Without this DC bias resistor, monitor output signal of breaking line will be about 0Vp-p. So when the normal monitor output signal rotate to the position which is detected as fault range, abnormality is detected by the square sum method.)

(3) Normal mode capacitor (C_N)

While basic circuit doesn't have C_N, it can improve electorical noise.

But the gain resistor(R_{IN}) and C_N work as filter, it cause one of factor of phase shift.

Time constant $=2\times((R_{IN}/2) // (R_{IN}/2)) \times C_N$

※ $(R_{IN}/2) // (R_{IN}/2)$ means parallel connection resistance value of $(R_{IN}/2)$ and $(R_{IN}/2)$.

This capacitor has an impedance$\{=1/(\omega \cdot C_N)\}$ and it affect signal level also.
Deviation of capacitor is much worse than that of resistor, please select the small deviation parts or small capacitance part to avoid impact of signal level.

(4) Common mode capacitor (C_C)

Standard usage is putting 1000p capacitor between S1~S4 signal and GND.

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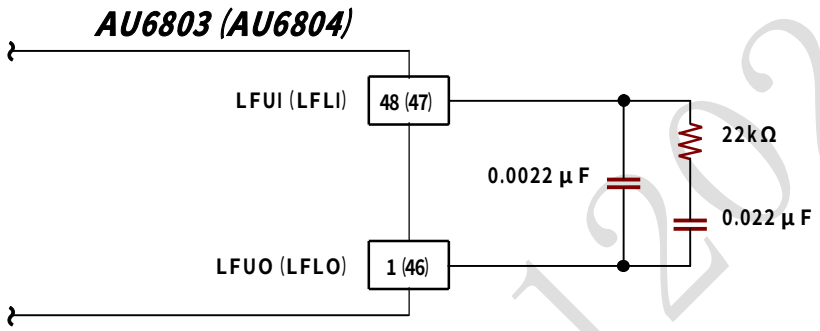
4.2.3 Loop Filter Circuit

In this product, loop filter circuit is one of the factors configuring the negative feedback control system to perform R/D conversion. To operate R/D conversion successfully, the electonic parts shown in below figure should be connected between "LFUI" and "LFUO" terminals, and "LFLI" and "LFLO" terminals respectively.

■Connection configuration of loop filter



Regarding loop filter connection, please connect wiring compact as much as possible with given the constant of resistor and capacitor. Especially input terminals (LFLI, LFUI) must be carefull not to enter noise due to sensitive terminals.
Also please select appropriate parts (especially capacitor) which meet required characteristic for temperature range.

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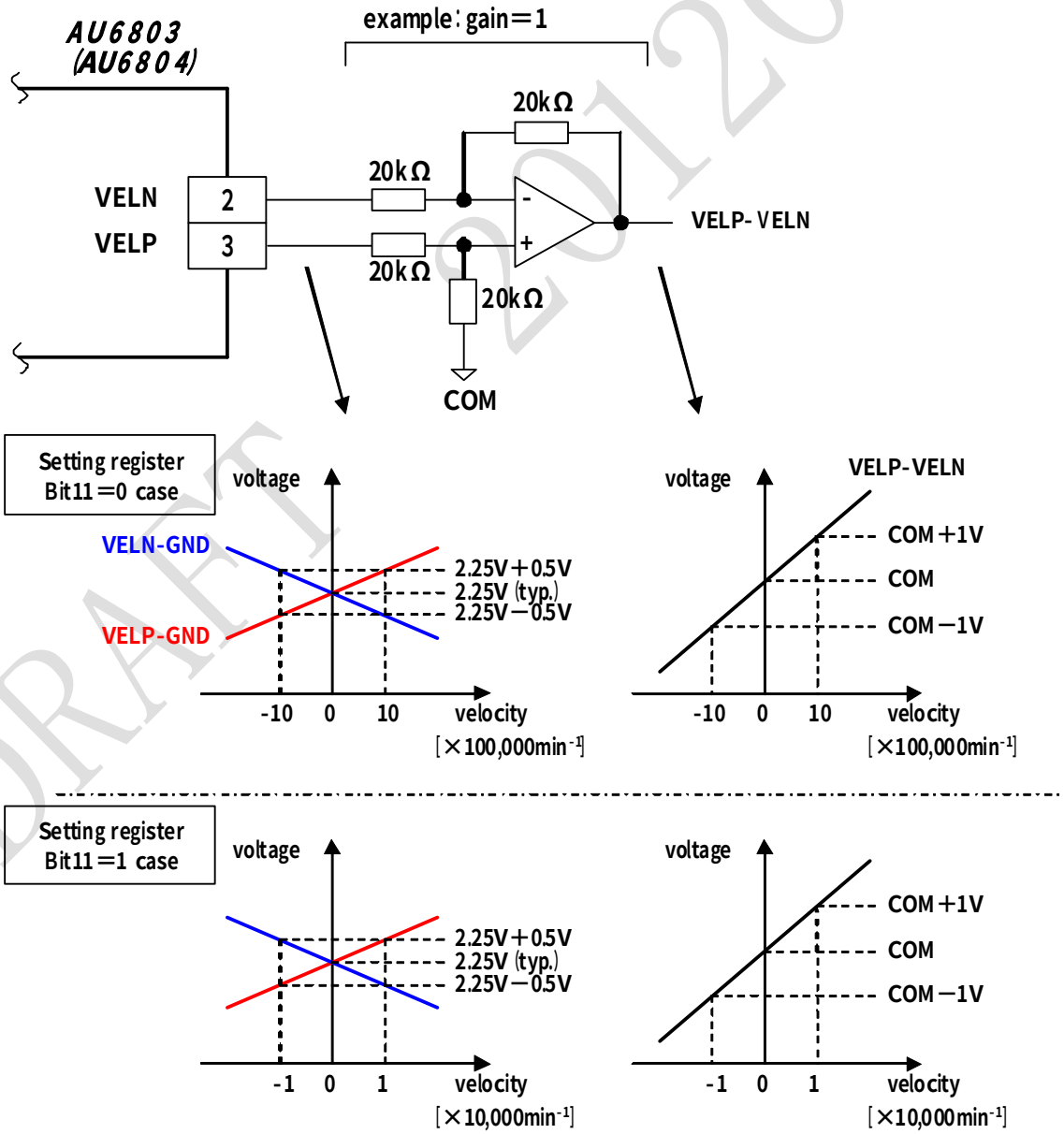
4.2.4 Analog velocity Output

■Considerations in analog velocity output

AU6803 (AU6804) has an analog velocity output terminal. But its accuracy is a rough so we do not recommend it for control.
Example of configuration register setting "Bit11＝1", (VELP－VELN)＝100 (typ.) [μV/min^{-1}], then "±10,000min^{-1}" means ideally "±1V (typ.)" output. But we can not get an accurate output cause of voltage offset [＝±2V (max.)] and gain error [＝-30%/＋20%] and temperature coefficient.

■How to use

The following is an example of the speed voltage output.



(Record) Velocity_Out＋Direction＝Digital_Out UP Direction

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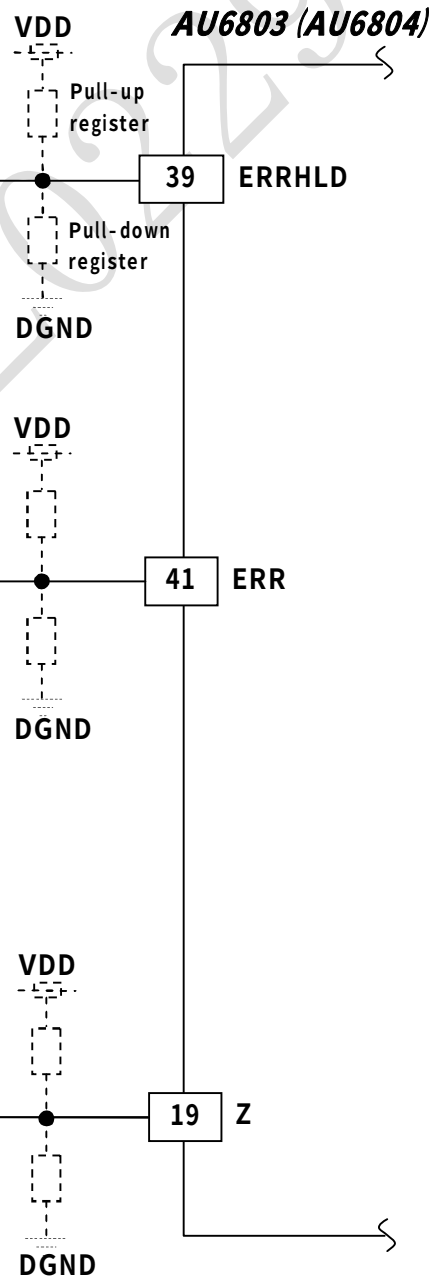
4.3 Digital Interface

4.3.1 Mode Setting･Function Selection

(1) Default setting

AU6803 (AU6804) has a mode-setting function(for below 3-pins) that detects the terminal voltage level as an input terminal at power-on, by means of adding a pull-up register of 10KΩ or a pull-down register of 10KΩ to the output terminals.
Please make the appropriate settings for each application in this function.



■**Output-mode setting**

	Pull-up (10kΩ)	Pull-down (10kΩ)
Output mode (D0－D11)	Absolute parallel angle data	Pulses equivalent to encoder

Parallel out pins (D0－D11) mode setting.
Refer section 2.2、4.3.2 (1) for actual description.
(Serial output is not covered by this setting.)

※This setting can be rewritten in the serial input configuration.
(Target setting register: Bit 1)

■**Oscillator selection for excitation**

	Pull-up (10kΩ)	Pull-down (10kΩ)
Oscillator	Internal oscillator	External clk input

Select the source of excitation output.
Internal oscillator: The IC's internal oscillator is used.
External clk: Use an external clock input.

Excitation frequency＝ Clk_frequency/1024

※This setting can be rewritten in the serial input configuration.
(Target setting register: Bit 2)

■**Excitaion output mode setting**

	Pull-up (10kΩ)	Pull-down (10kΩ)
Excitation mode	Current excitation mode (VMD＝0)	Voltage excitation mode (VMD＝1)

Reference waveform (Current waveform between R1-R2), and Resolver signal input (SINMNT, COSMNT pin waveform), Select appropriate mode by checking phase difference of above.

■Phase difference＝＋90°±45° -→ Current excitation mode (VMD＝"0")
■Phase difference＝ 0°±45° -→ Voltage excitation mode (VMD＝"1")

※If this mode setting is incorrect, digital output angle value will shift 180 degree.
※This setting can **NOT** be rewritten in the serial input configuration.

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(2) Serial input setting

AU6803 (AU6804) has a function that makes it possible to change the contents of the setting register shown in below table through the serial input. At this function, it is possible to set right operation mode for individual applications, and set the content in diagnostic of BIST function.

※The "SSCS" input terminal should be connected to the power supply(VDD) when this function is not used.

■Description of serial input setting register

<table>
<tr><th>Bit NO.</th><th>Items</th><th>Description of Setting</th></tr>
<tr><td>1</td><td>Setting of output mode
(D0～D11)</td><td>[0] : Absolute value (φ1～φ12) of parallel angle data.
[1] : Pulses equivalent to Encoder (A,B,Z,U,V,W)</td></tr>
<tr><td>2</td><td>Selection of operating clock</td><td>[0] : Internal oscillator
[1] : External clock input</td></tr>
<tr><td>3
4</td><td>Setting of serial output mode
[Bit 4,3]</td><td>[00] : Absolute value (φ1～φ12) of angle data
[01] : Pulses equivalent to Encoder (A,B,Z,U,V,W)
[10] : Serial call-back (For checking the setting register)
[11] : Result of failure detection/BIST</td></tr>
<tr><td>5
6</td><td>Signal setting of Pin No.44 & Pin No.22
[Bit 6,5]</td><td>
<table>
<tr><th></th><th>Pin No.44</th><th>Pin No.22</th><th rowspan="5">Please use the default value for Bit5、6 .</th></tr>
<tr><td>[00]</td><td>Z output
(Zero point pulse output)</td><td>PRTY output
(Parity output)</td></tr>
<tr><td>[01]</td><td>Test output 1</td><td>Test output4</td></tr>
<tr><td>[10]</td><td>Test output 2</td><td>Test output5</td></tr>
<tr><td>[11]</td><td>Test output 3</td><td>Test output6</td></tr>
</table>
</td></tr>
<tr><td>7
8
9
10</td><td>Setting of built-in self-test
(BIST)
operation
[Bit 10,9,8,7]</td><td>[0000] : BISTVLD (Input) invalid
[0001] ～ [0100] : Reserved (Do not select this code.)
[0101] : BIST of R/D conversion : Command angle 1 (0 °)
[0110] : BIST of R/D conversion : Command angle 2 (45 °)
[0111] : BIST of R/D conversion : Command angle3 (270 °)
[1000] : Reserved (Do not select this code.)
[1001] : Reserved (Do not select this code.)
[1010] : BIST of failure detection : BIST of breaking of wire detection for COS signal line.
[1011] : BIST of failure detection : BIST of breaking of wire detection for SIN signal line.
[1100] : Reserved (Do not select this code.)
[1101] : System Reset
[1110] ～ [1111] : Reserved (Do not select this code.)</td></tr>
<tr><td>11</td><td>Setting of VEL output range
(Analog velocity)</td><td>[0] : 10 μV/min^{-1} (0 ～ 240,000min^{-1})
[1] : 100 μV/min^{-1} (0 ～ 24,000min^{-1})</td></tr>
<tr><td>12</td><td>Setting of threshold value for abnormal square-sum</td><td>[0] : 0.7 Vp-p
[1] : 1.0 Vp-p</td></tr>
</table>

※ The default value setting is zero (0) for all bits except the specification of 4.3.1 (1) .

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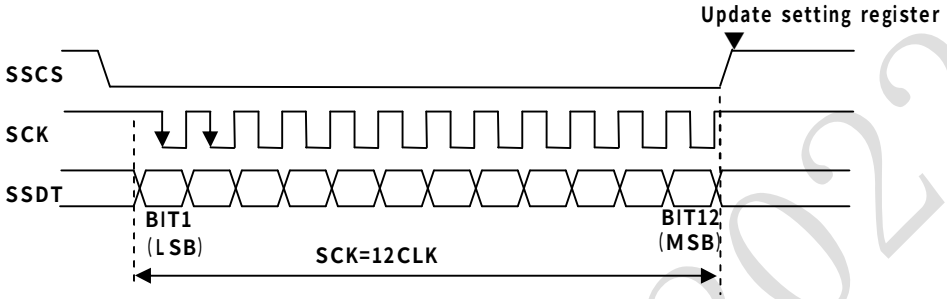
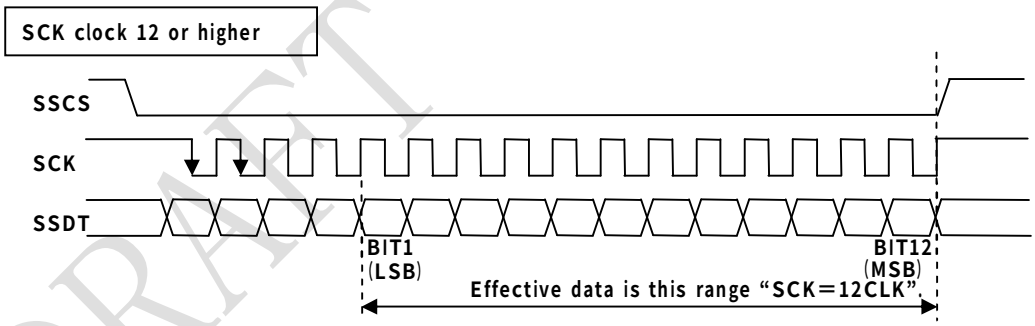
■Setting method

Serial input operation is controlled by SSCS/SCK/SSDT pins. SSDT data will be entered by synchronized timing to SCK input at the active condition of SSCS input "L" level. Please switch the SSDT input at the rising edge of SCK, while SSDT data will be incorporated at the falling edge of SCK.



※Refer 10.9 to check each signal timing.

Note, when SCK clock number is greater than 12 while SSCS="L", effective data will be last 12 one of the last 12 SCK.



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4.3.2 Output Interface

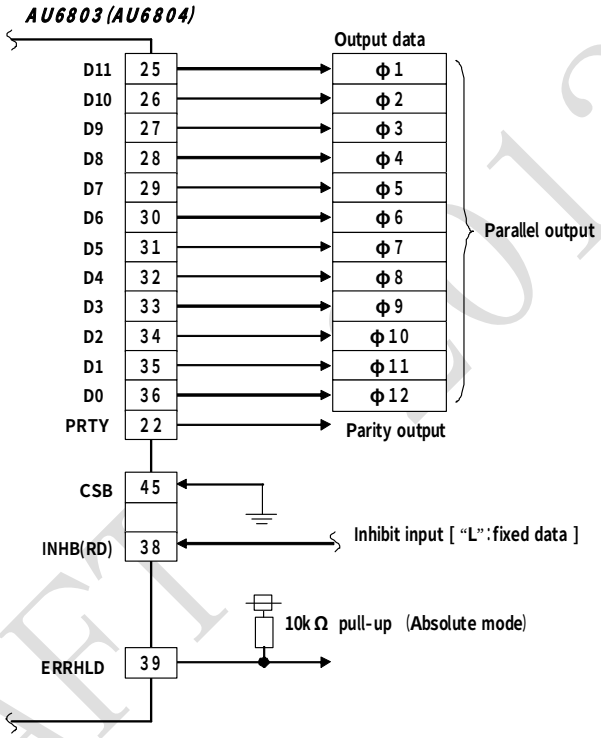
(1) Parallel output

Examples of parallel output are as follows. Note that it assumed to make parallel output mode setting by default setting (refer 4.3.1(1)) in this chapter. It is also OK to use serial input setting (refer 4.3.2(2)).

■ Usage of Absolute output mode

—(stand-alone) usage : Interfaced by dedicated I/O—

When it use in standalone, CSB pin must be "L" lebel. And please read "φ1~φ12" data which control through/hold by INHB(RD) pin.



※ Please refer chapter 10.9 for φ1～φ12、PRTY、CSB、INHB timings.

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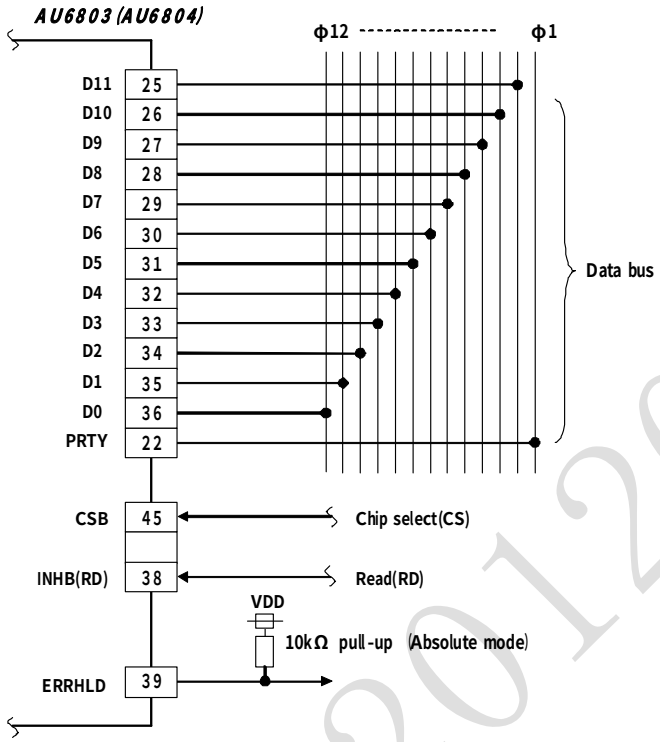
—《Bus interface》 usage ： Interfaced by BUS line—

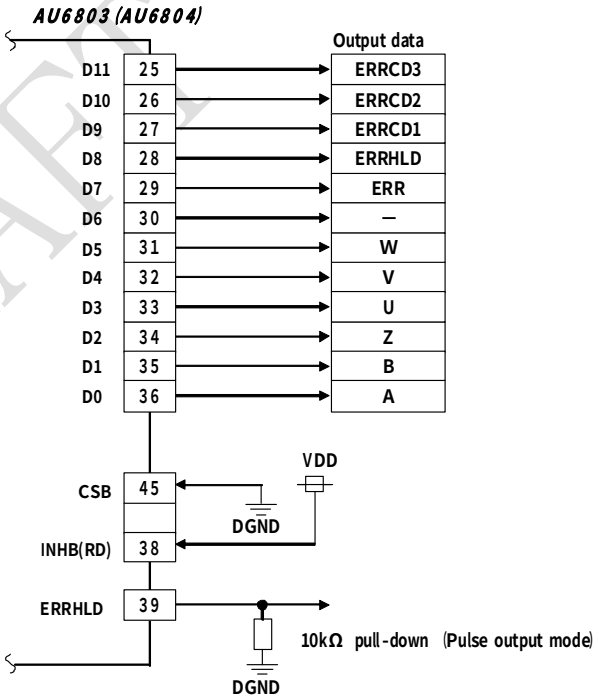
When it use in bus line, D0～D11 and PRTY output state must be controlled by CSB pin. And please read "φ1~φ12" data which control through/hold by INHB(RD) pin.



※ Please refer chapter 10.9 for φ1～φ12、PRTY、CSB、INHB timings.

■Usage of Pulse output mode

When it use in pulse output mode equivalent to an encoder, Set CSB="L" and INHB(RD)="H".



※ A,B,Z pulse which come from D0~D2 pins are same signal with dedicated A,B,Z pin (42~44 pin).

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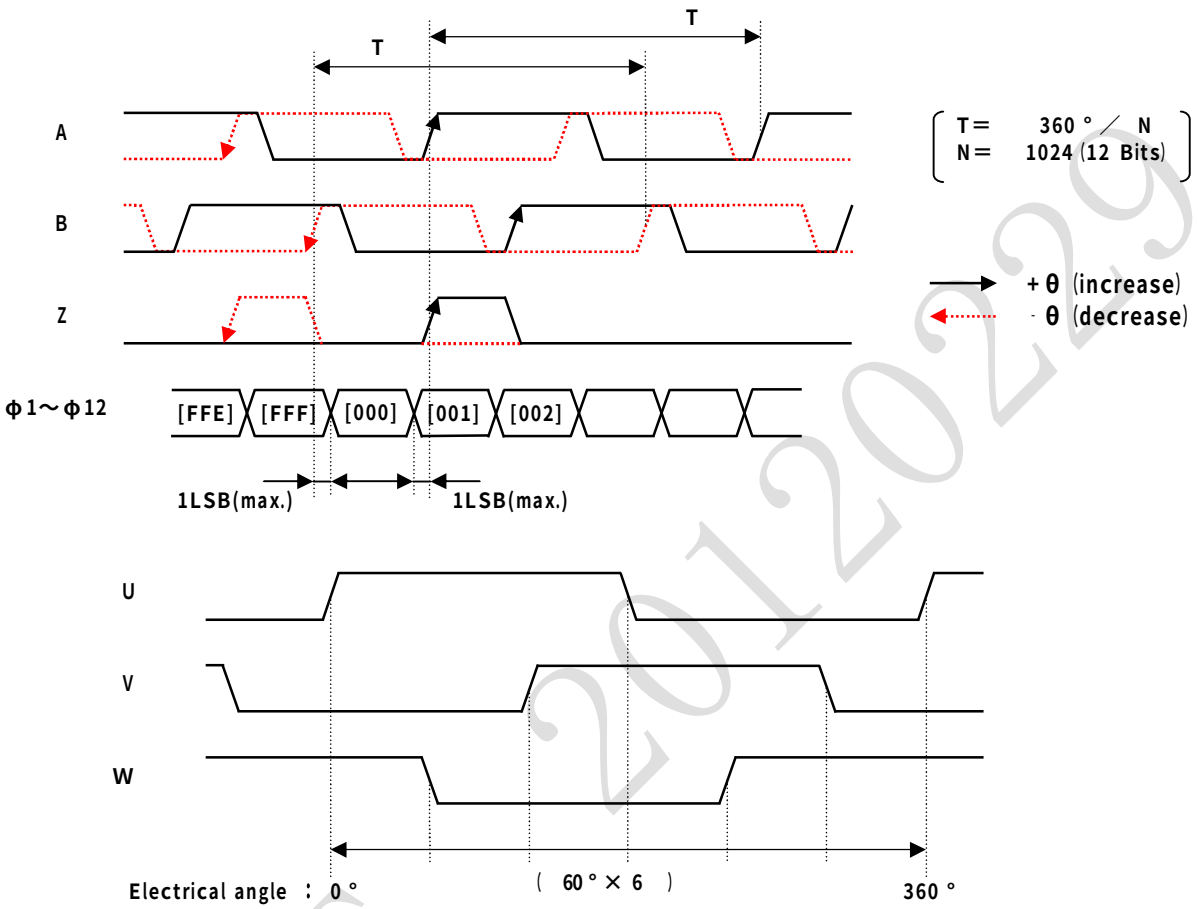
—Pulse output equivalent to an encoder—

The waveform of pulse output is shown below.



※The pulses output equivalent to an encoder have a 1-bit hysteresis circuit to prevent chattering. Then there might have deviation against absolute angle data according to resolver rotation direction.

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(2) Serial output

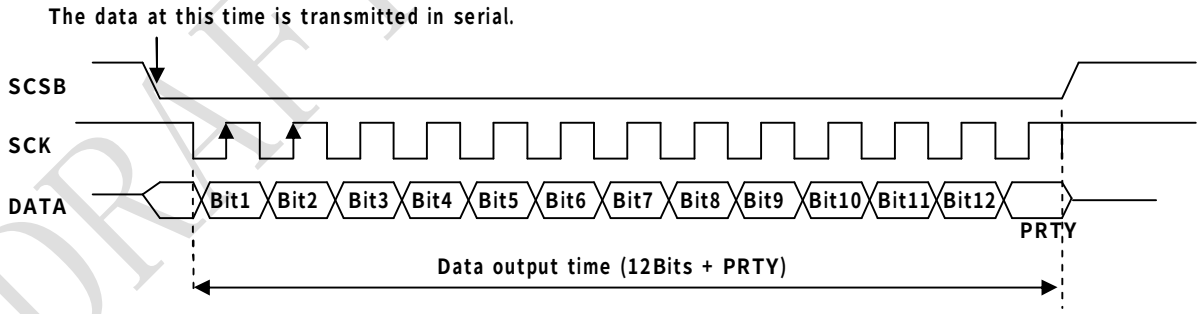
This IC has a serial output data selection function that is defined by mode setting (Bit4, 3) of serial input setting register. Each serial output mode setting shows below output signals.

■Description of serial output signal

Serial output mode setting [Bit 4,3]	Bit No. of "DATA" output											
	1	2	3	4	5	6	7	8	9	10	11	12
Setting [00]: Absolute output mode	LSB Φ12	Φ11	Φ10	Φ9	Φ8	Φ7	Φ6	Φ5	Φ4	Φ3	Φ2	MSB Φ1
Setting [01]: Pulse output mode	Pulses equivalent to Encoder						-	ERR	ERR HLD	ERR CD1	ERR CD2	ERR CD3
	A	B	Z	U	V	W						
Setting [10]: Serial call-back	Setting Bit 1	Setting Bit 2	Setting Bit 3	Setting Bit 4	Setting Bit 5	Setting Bit 6	Setting Bit 7	Setting Bit 8	Setting Bit 9	Setting Bit10	Setting Bit11	Setting Bit12
Setting [11]: Results of BIST	Default Bit 1	Default Bit 2	BIST CD1	BIST CD2	BIST CD3	BIST CD4	During BIST operation	VMD	ERR HLD	ERR CD1	ERR CD2	ERR CD3

■Usage

Serial output is controlled by SCSB/SCK pins. Serial data output from DATA pin with synchronized timing to SCK input at the active condition of SCSB input "L" lebel. DATA output switch at the falling edge of SCK, so please read output serial data at the rizing edge of SCK essentially.



※Please refer chapter 10.9 for each signal timing.

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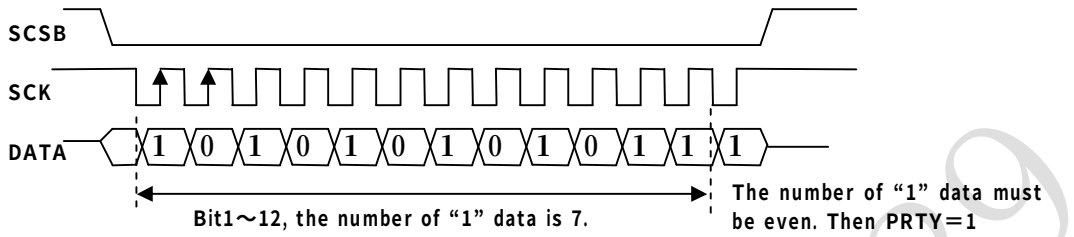
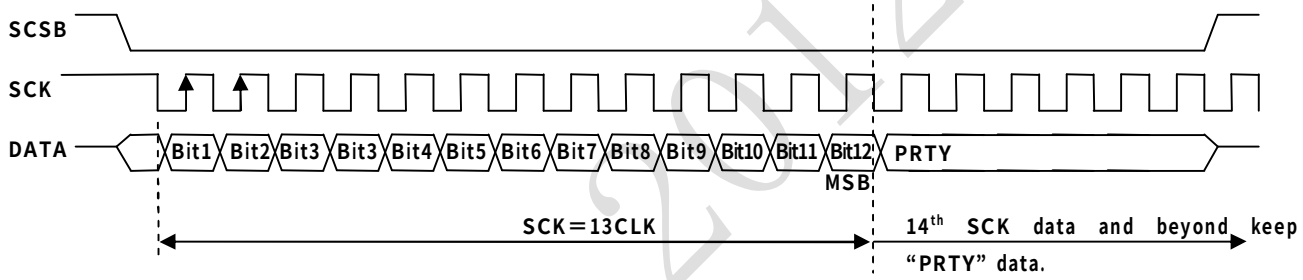
Note, PRTY is defined as even parity. The number of "1" data between serial data "Bit1~12" and "PRTY" must be even.

Example



Also while SCSB＝"L" fix and "SCK" clock keep to enter, 14th SCK data and beyond shows "PRTY" data.

More than 14 sck case.



■Considerations for using the serial output

When using the serial output feature, please note the following points.

① In serial output, required time to transmit all bits may generate some dead time in the control system. Especially it is possible to recognize the present position with some error in case of using the pulse output equivalent to an encoder.

② The effected signals by INHB are absolute output φ1～φ12, PRTY, pulse output equivalent to encoder U, V, W, and ERR, ERRHLD, ERRCD1～3 .

③ In case of changing from the serial output mode(except absolute output mode) to absolute output mode like described below, please follow next page sequence.

[Pulse output mode]
Bit [4,3] = [0,1]
[Serial call-back]
Bit [4,3] = [1,0]
[Results of BIST]
Bit [4,3] = [1,1]

⇒ [Absolute output mode]
Bit [4,3] = [0,0]

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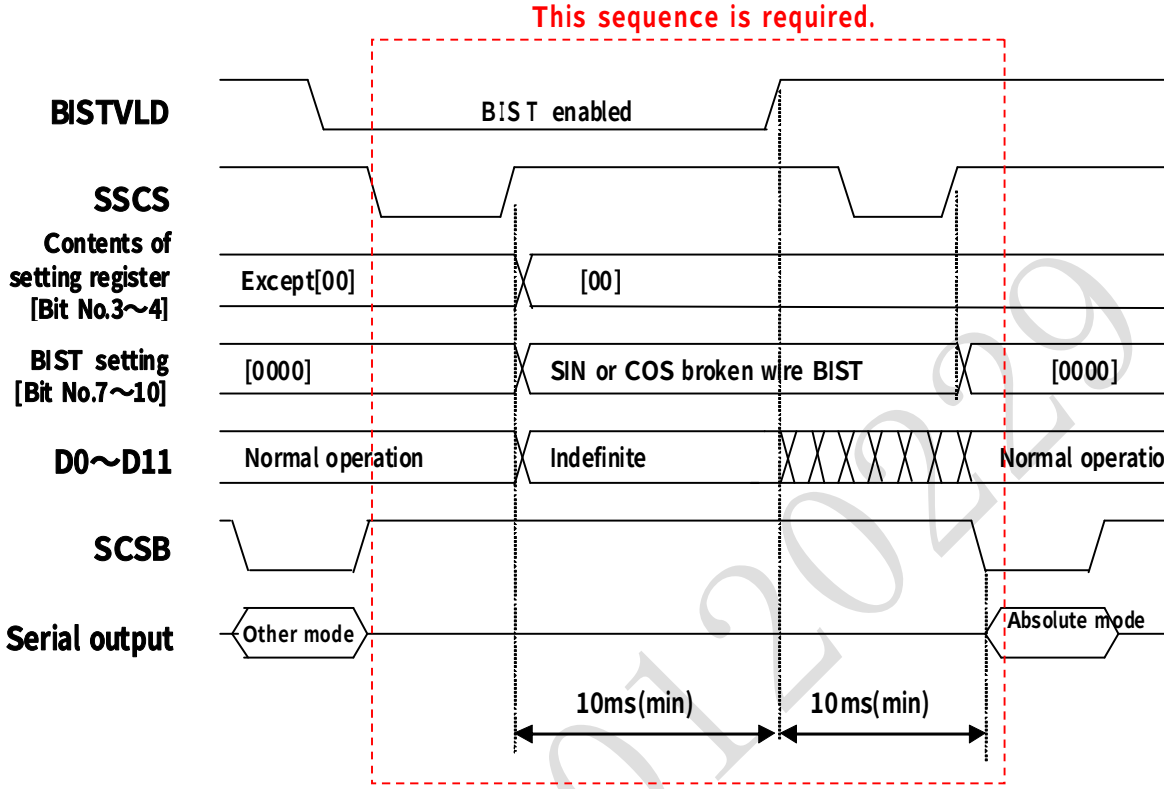

※Above contents corresponds specification P6 figure3-1.

(3) A, B, Z independent pin output

A/B/Z pin (42~44pin) output the pulses equivalent to an encoder A/B/Z phase respectively. These independent output terminals are same signal with parallel output mode D0~D2. Please refer chapter 4.3.2(1) for signal timings, etc.

※A/B/Z independent outputs are outside the scope of the CSB input.

(4) Use verbose output

Each output signals described in 4.3.2(1)~(3) can use a combination of more than one signal.
Example the absolute value can be detected by using serial output and A/B/Z signals. Serial (absolute mode) data load after power on, and then absolute data can be caliculated by count up/down with A/B phase. It need total 6 I/O pins which mean 3 pins for serial and 3 pins for A/B/Z then you can reduce the I/O of the CPU. It can also be used for fault detection of digital output system by the combination of parallel output and serial output.
To suit individual applications and requirement, please utilize this verbose function.

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4.3.3 Clock for Excitation

There is an clk selection mode described in 4.3.1 (1) default setting or 4.3.1 (2) serial setting. An excitation clk can be generated from internal oscillator or external clock.

(1) Selection of internal oscillator

Using the IC's internal oscillator, then it does not need external clock. CLKIN:17pin (external clock) should be open.

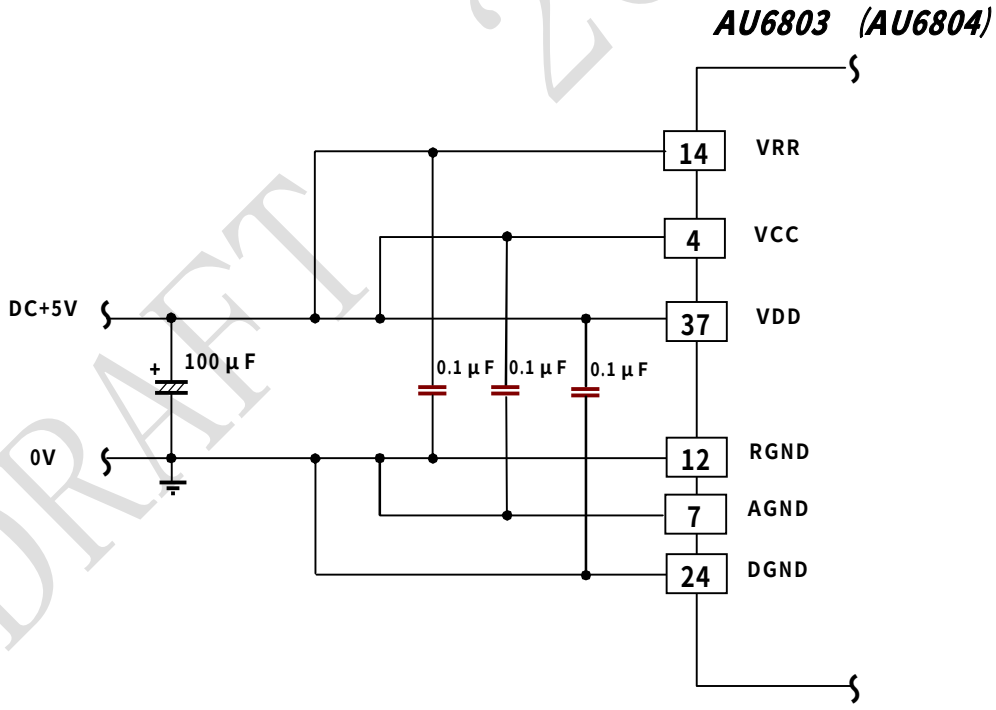
(2) Selection of external clock

This is useful to set the desired frequency of the excitation frequency. External clock should be input to CLKIN:17pin. This is TTL-level pin.

Excitation frequency＝(External clock frequency)/1024

※ An external clock can be getting to be noise source. Then its board pattern must be as short as possible with guard GND pattern in order to make effective EMC measures.

4.4 Power Source



Power source is single supply +5V±5%. Analog power lines(VCC/AGND), digital power lines (VDD/DGND) and excitation power lines (VRR/RGND) must connect to each of the same one.
If you set separate power line for VCC-VDD－VRR or AGND-DGND－RGND, there must be no potential difference and power switching(On/Off) should be done simultaneously.
Above figure is example of power connection. Regarding 0.1uF capacitors, it should be located close to AU6803(AU6804) device as much as possible.

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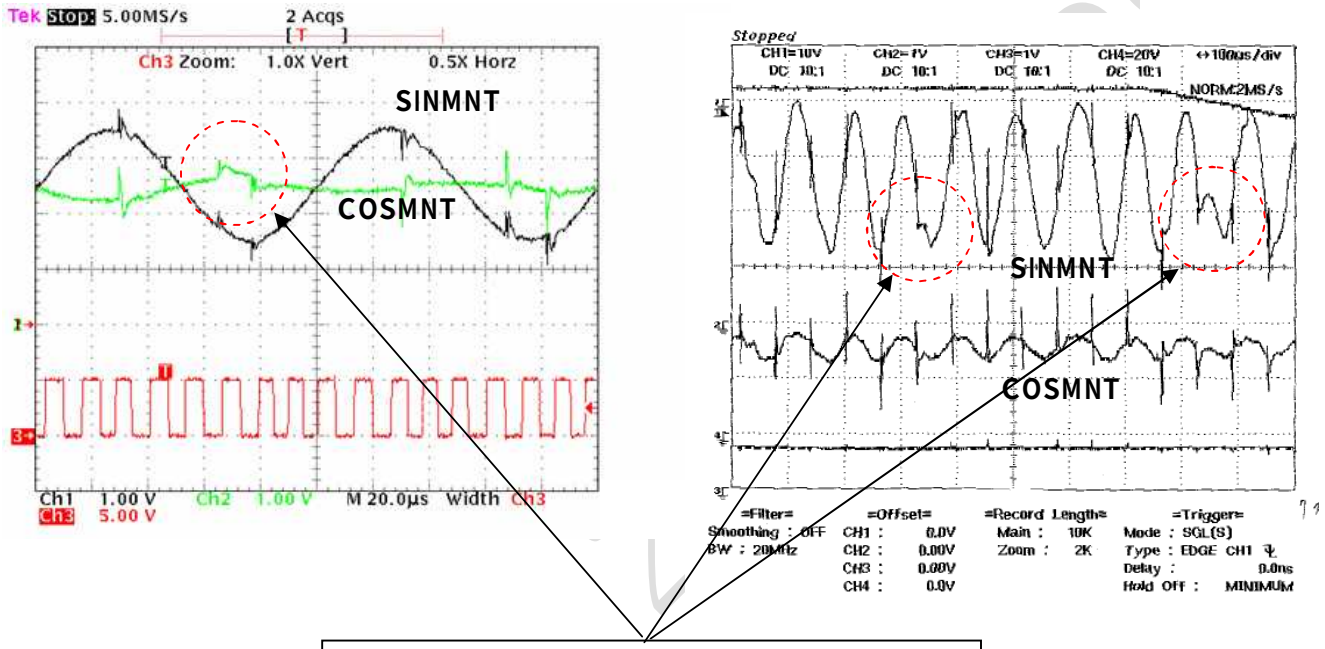
4.5 Countermeasures for Noise

Below waveforms are measured actually. Countermeasure for noise must be done in accordance with the specification P28 contents.

■Waveforms of magnetic noise

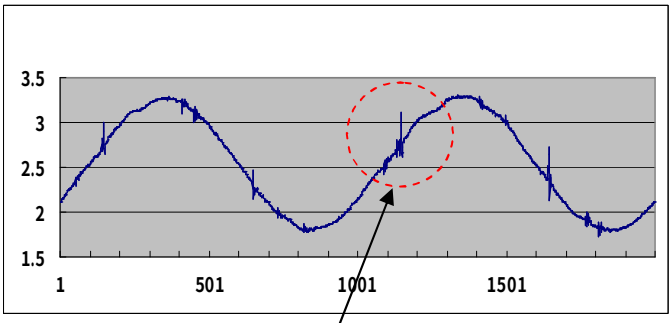
Magnetic noise happens when the leakage flux of the motor passes through the resolver. Its effect will be bigger turbulence of digital output, which will generate error.



Basic waveform (10kHz) deformed.

■Waveforms of electrical noise

Electrical noise happens when the spike noise caused by PWM drive of the motor affects signal lines. Turbulence of digital output will not be so big but it will generate error depend on the size of noise.



Basic waveform (10kHz) was not changed much.
But spike noise was overlapped.

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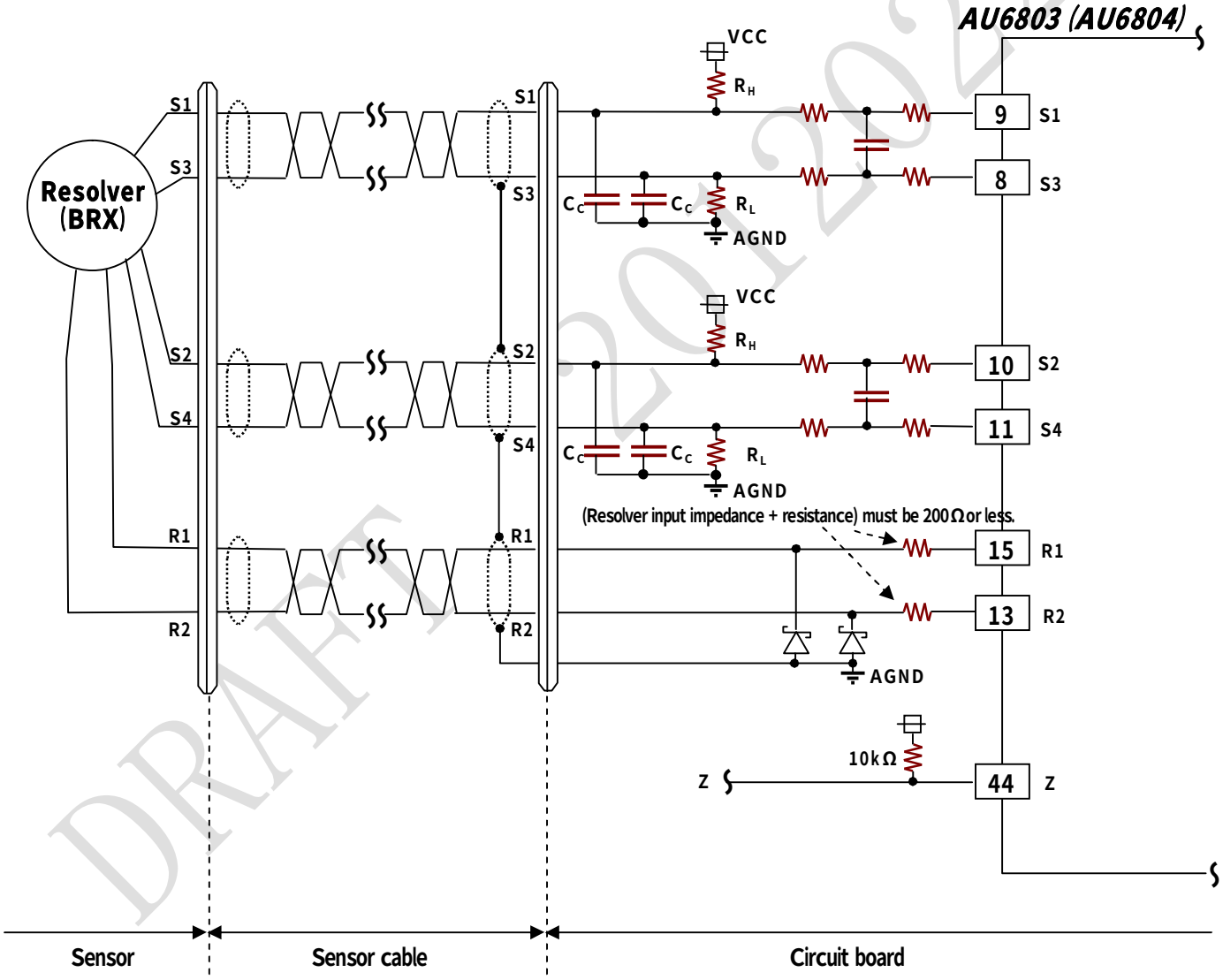
5. Connection

Caution !

Please take off the power during connection operation. After power off, take enough time, check the voltage value by tester, and please operate wiring and connecting.

5.1 Example of Resolver Connection

■ **Connenction and configuration example using direct excitation functions of this product.**



Resolver signals S1/S2/S3/S4 connects AU6803(AU6804) terminals S1/S2/S3/S4 each via the resolver signal input circuit. And resolver signal R1/R2 connects AU6803(AU6804) R1/R2. R1/R2 line will have series resistance and schottky barrier diode to measure noise inflow from resolver excitation line. When used in an environment with no surge they are not needed and will be no problem at function view point. At this direct excitation mode, normally use current excitation mode so please add 10kΩ pull-up resistance for Z terminal.

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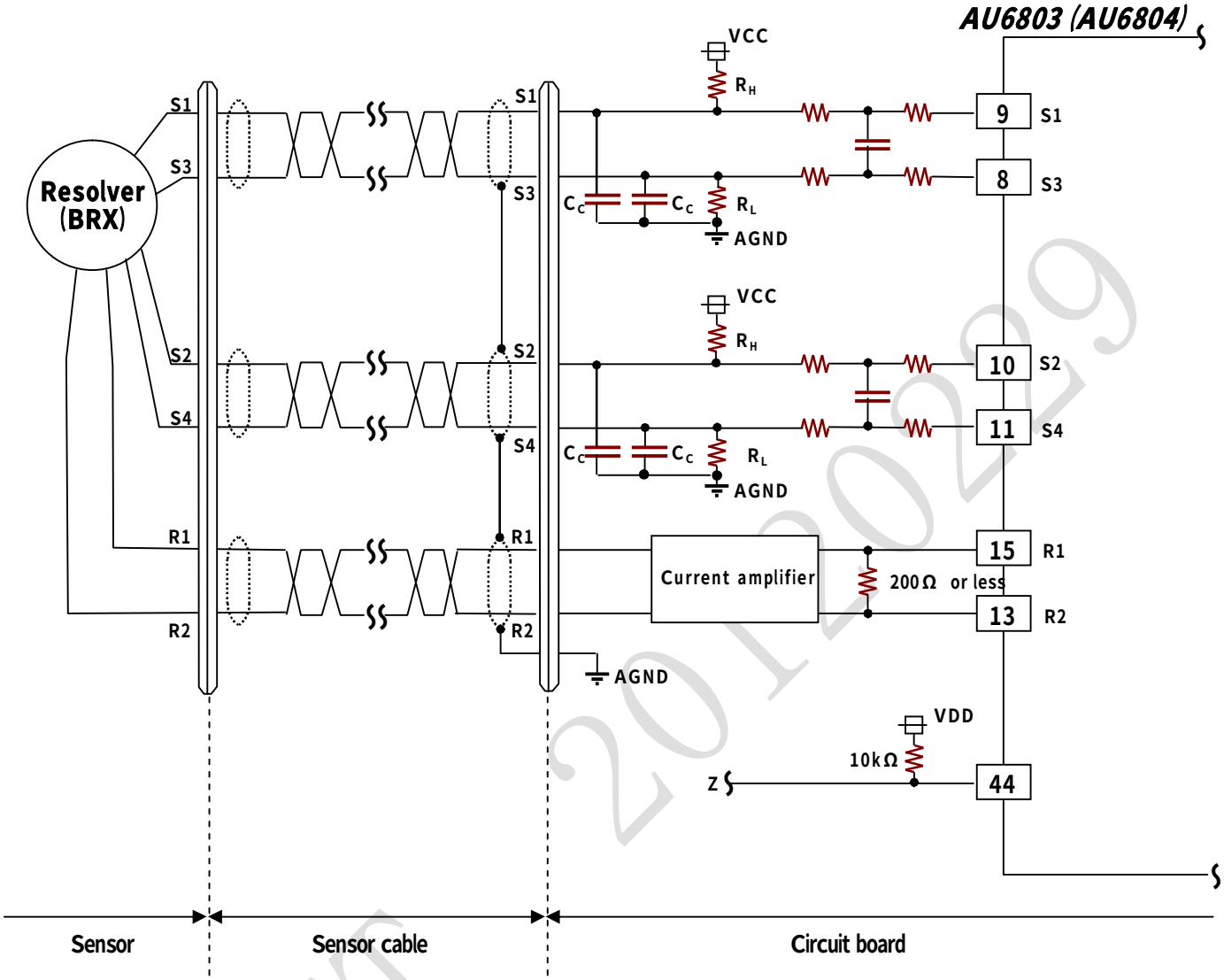
■ Connenction and configuration example using external current amplifier to excite resolver



Resolver signals S1/S2/S3/S4 connects AU6803(AU6804) terminals S1/S2/S3/S4 each via the resolver signal input circuit. The voltage generated across the resistor connected between the terminal of AU6803(AU6804) R1 and R2 is getting to be source of current amplifier. The resolver R1/R2 signals connect to this current amplifier output terminal. When a resolver is excited by external current amplifier like this, normally use current excitation mode so please add 10kΩ pull-up resistance for Z terminal.

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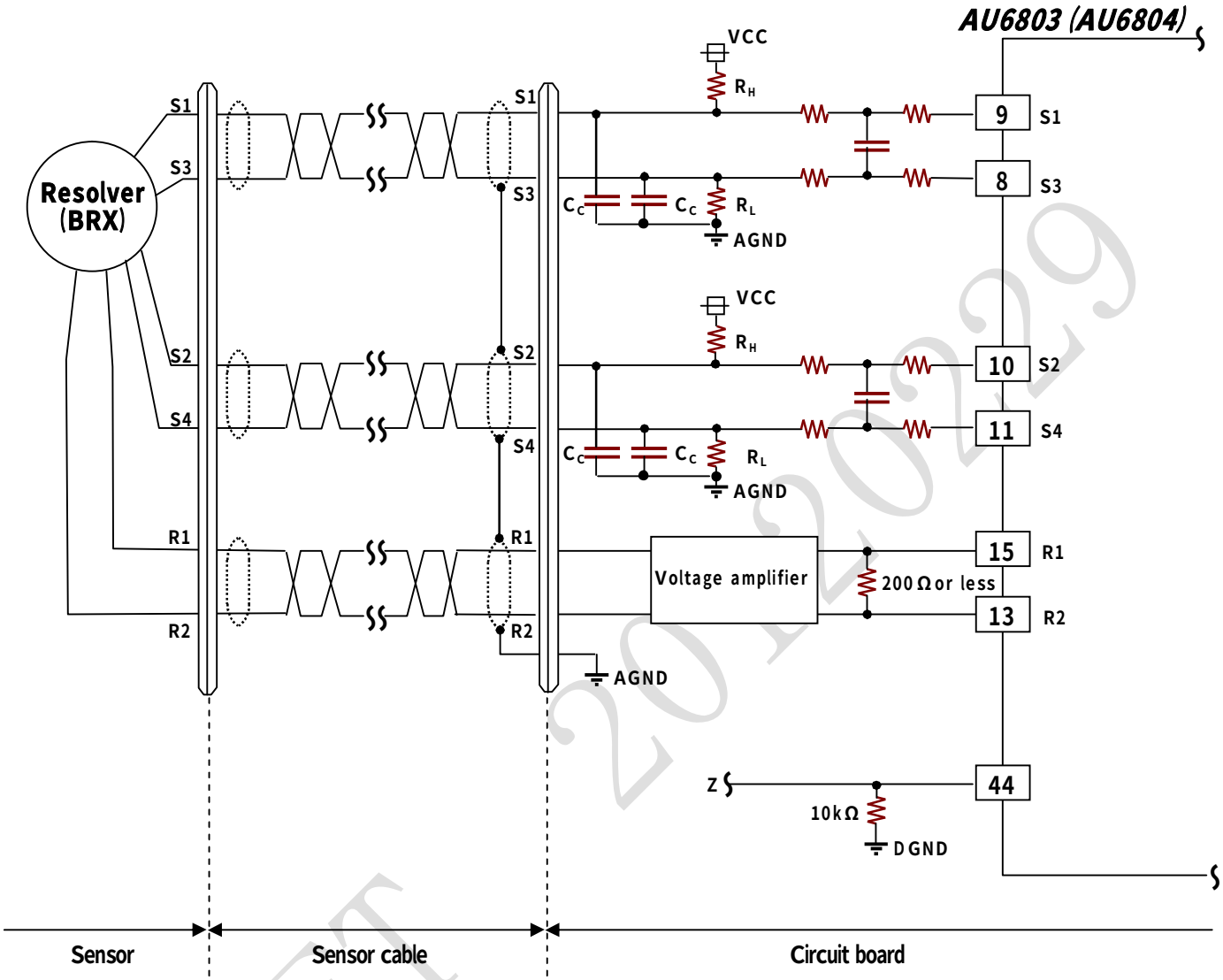
■ Connenction and configuration example using external voltage amplifier to excite resolver



Resolver signals S1/S2/S3/S4 connects AU6803(AU6804) terminals S1/S2/S3/S4 each via the resolver signal input circuit. The voltage generated across the resistor connected between the terminal of AU6803(AU6804) R1 and R2 is getting to be source of voltage amplifier. The resolver R1/R2 signals connect to this voltage amplifier output terminal. When a resolver is excited by external voltage amplifier like this, normally use voltage excitation mode so please add 10kΩ pull-down resistance for Z terminal.

※ (To an AU6802N1 experienced user)
AU6803 (AU6804) resolver signal input circuit have different with AU6802N1 case. Note that A connextion polarity of DC bias resistor(R_H、R_L) for disconnection detection resolver signal is reversed.

5.2 Example of Power Connection

Refer the section 4.4

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6. Check Point of Operation

Before power-up, please make sure that the connections are no problem.

6.1 Check Point for Resolver Interface

6.1.1 Check Point of Excitation Signal

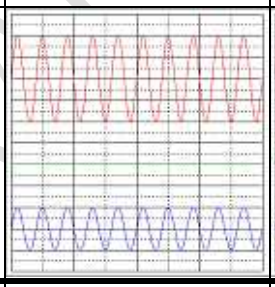
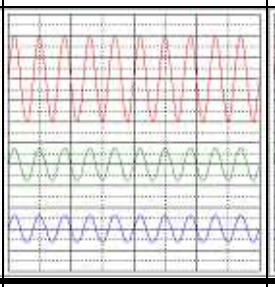
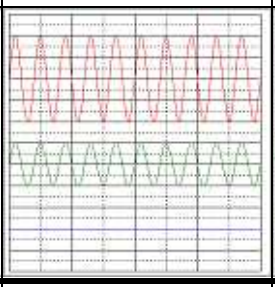
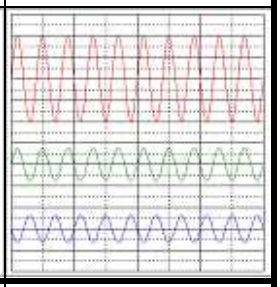
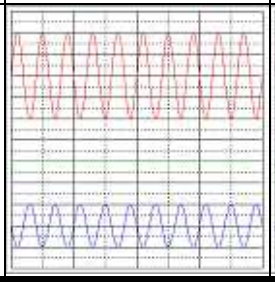
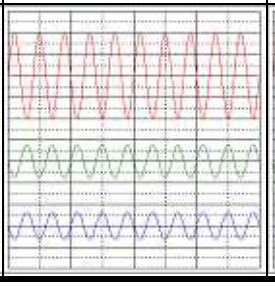
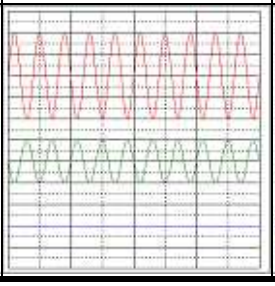
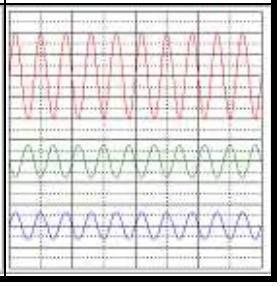
Check your resolver excitation signals (R1, R2) whether the resolver is excited with your designed amplitude or not. If signals are small or saturated situation, please check the suitability of the load and excitation circuit which connect to AU6803(AU6804) excition output terminal again. If there are no signals, please check the connection to resolver and power supply status.

6.1.2 Check Point of Monitor Signal Amplitude

(1) Check point of amplitude change

Observing the waveform of resolver exciting signals and monitor output (SINMNT、COSMNT), please check if the monitor output have a same frequency carrier of excitation signals. After then, rotate the resolver, please check that monitor signal amplitude is changing with corresponding resolver angle. If there is no signal or no amplitude change by rotation, please check the connection between resolver and AU6803(AU6804).

■Waveform example of exciting signal and monitor signal with some fixed angle

Electrical angle	0 °	45 °	90 °	135 °
Excitation signal SINMNT COSMNT				
Electrical angle	**180 °**	**225 °**	**270 °**	**315 °**
Excitation signal SINMNT COSMNT				

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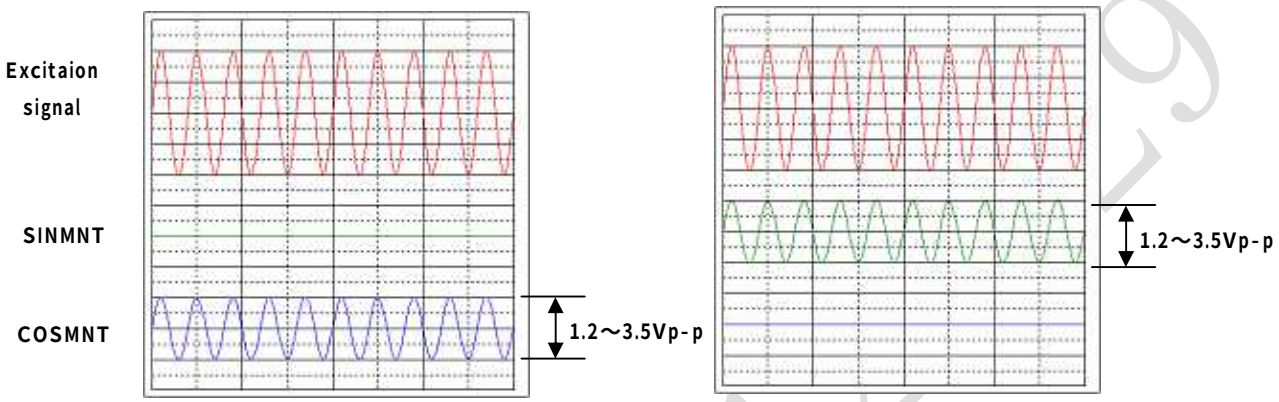
(2) Check point of amplitude level

Rotating the resolver with observing a monitor signal, please check the monitor signal (SINMNT and COSMNT) maximum amplitude In case of 1.2~3.5Vp-p monitor amplitude range, you can get specification performance of this product. If signal amplitude is not appropriate range, please adjust your circuit constants of exciting amplifier and resolver signal input circuit.



6.1.3 Check Point of Phase Shift

Rotating the resolver with observing a exciting current output(R1-R2) of AU6803 (AU6804) and a monitor output voltage waveform, Please check the phase difference between a excitation waveform component of R1-R2 current output and a excitation waveform component of the output voltage monitor while both measurement signals are same phase. And measuring phase difference must be inside below range of setting excitation-mode. When that is outside the acceptable range, please set an appropriate excitation-mode to make phase difference inside the acceptable range.

Setting of excitation mode	Phase shift acceptable range
Current excitation mode (VMD="0")	+90 ° ±45 °
Voltage excitation mode(VMD="1")	0 ° ±45 °

※ Regarding AU6803 (AU6804) definition of phase shift, please note that the current phase is a criteria and it is not for voltage phase difference between excitation signal output terminals (R1-R2).

■How to check the current phase excitation output

When you check the current phase of AU6803(AU6804) excitation output(R1-R2) by oscilloscope, please prepare current probe. Otherwise you can confirm it by the following methods which fit for each excitation mode.

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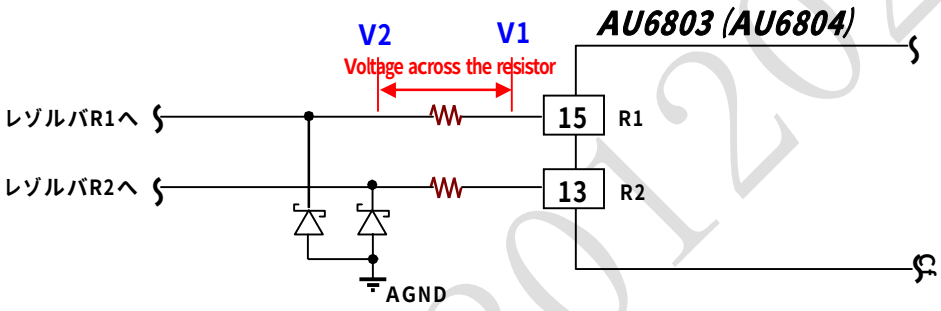
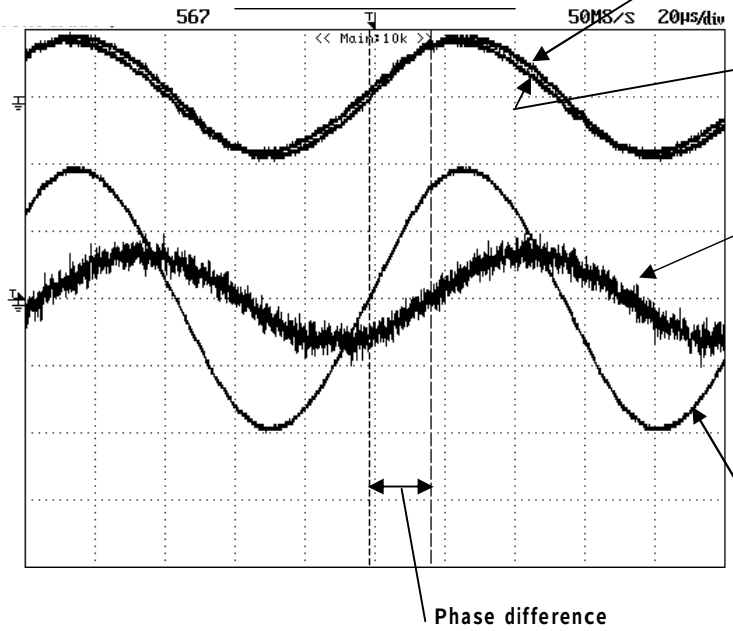
Caution !	If the R1 or R2 terminal is short-circuited to GND or the power line(VRR/VCC/VDD etc) may cause damage. When the waveform between R1 and R2 need to be checked, observe it as the difference of each waveform. Never connect probe-GND directly to the R1 or R2 terminal.

(1) In case of using direct excitation function(Current mode) of this product.

If R1/R2 lines have series resistance and schottky barrier diode to measure noise inflow from resolver excitation line, you can measure the voltage phase across the resistor inserted in series as the desired current phase. Then you can see the current phase with measuring the voltage waveform across the resistor in series either.



Example waveform



※The above example is for the phase advance case of voltage monitor signal.

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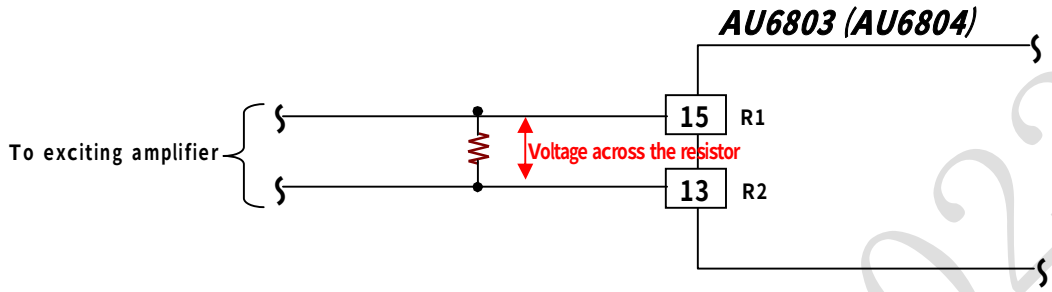
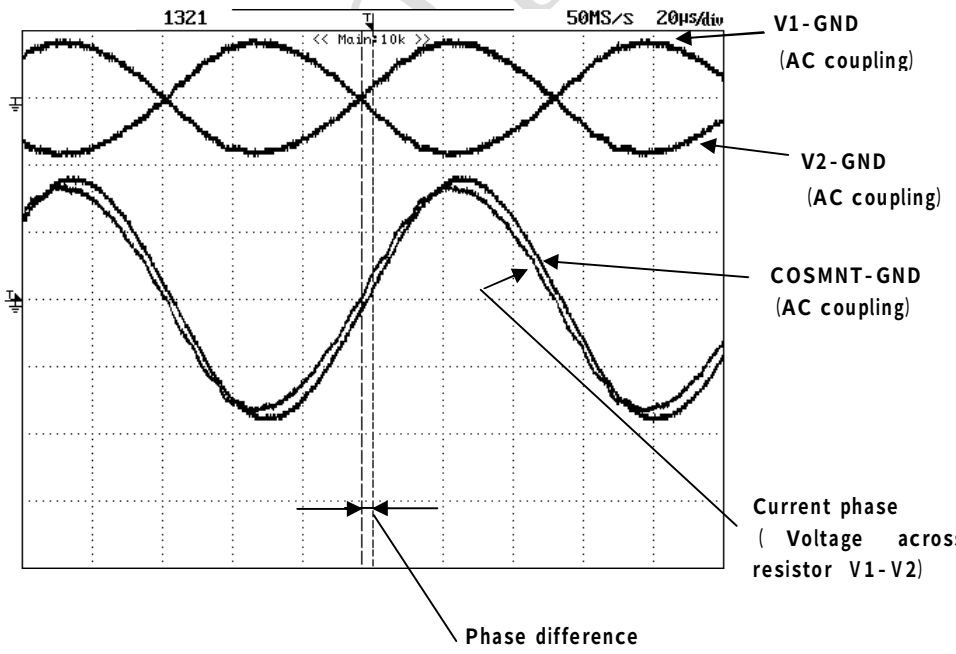
(2) In case of using external amplifier to excite resolver.

An external excitation amplifier (either voltage-type and current-type) need input as voltage source which is converted from exciting current output of AU6803(AU6804) by inserting a resistor between R1 and R2 like below. Then this voltage phase of across the inserting resistor is getting to be same as the desired current phase. So you can get the current phase with measuring the voltage waveform across the inserting resistor.



Example waveform



※The above example is for the phase delay case of voltage monitor signal.

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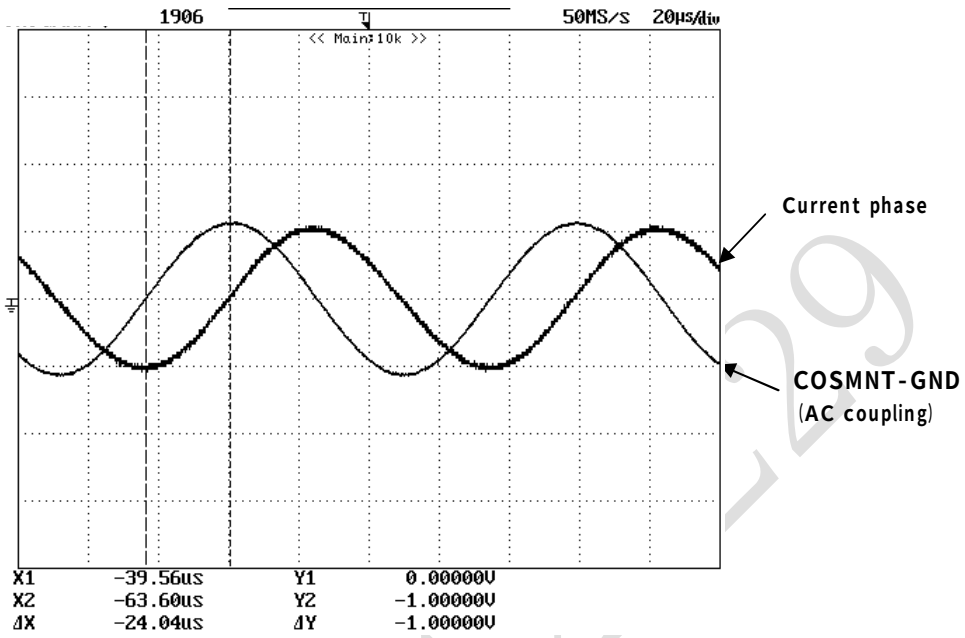
■How to convert an angle of phase shift



Phase shift [°] =360 [°] × (Time shift [µs] ／Exciting frequency period [µs])

Above case：Exciting frequency=10kHz → Period=100µ (=1/10kHz)
Time shift =24µs
Phase shift=86.4 ° (=360×24／100)

6.2 Check Point for Digital Output

6.2.1 Check Point of Output Angle

Please check that the each digital output show your required format which you set and angle output data is changing with resolver rotation. If angle output is not change while resolver rotation or output format is different with your setting, please check a polarity of each digital input terminal. Also if output angle data does not match with actual angle or output data is not stable, refer section 6.1 and please check if there is no problem for resolver related connections.

6.2.2 Check point of abnormality Detection

"ERR" output and "ERRHLD" output should be both L-level for normal condition while "ERRSTB" input is H-level. If this device detects some error condition, "ERR" output or "ERRHLD" output will be H-level. Then you may refer section 9.1 and please isolate the true cause of the error and remove it.

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7. Built In Self Test (BIST) Function

AU6803 (AU6804) has a built-in self test function and you can determine the validity of operation by excuting this BIST function sequence. The details of the diagnosis are described below.

- BIST of R/D conversion : Self-diagnosis function of R/D conversion. It is self tested by means of the electrical angles of 0, 45 or 270 degrees set as the resolver signal input.

- BIST of failure detection : Self-diagnosis function of failure detection. Set the simulated abnormal conditions and possible to determine the validity of the failure detection operation. It include below.

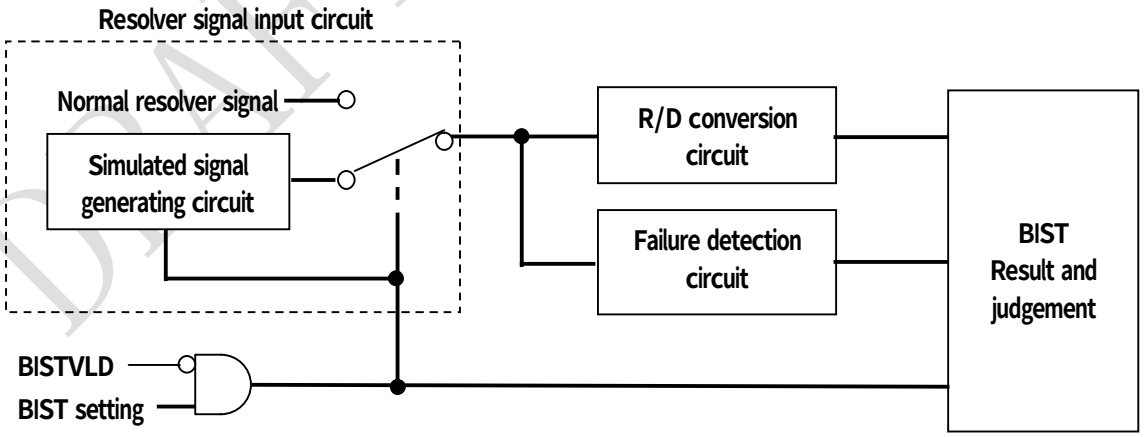
  ■ BIST of Broken Wire : Self-diagnosis for the detection function of a "Breaking of Resolver Signal Line"

In this section, we explain the operation, how to excute, and diagnostic results of BIST.

7.1 Run-Time Behavor of BIST

BIST functions test to determine the validity of the failure detection function by generating a required failure signal inside IC and monitoring the output signal. While each BIST is executing, device operations which is R/D conversion and failure detection are switched to work on simulated signal base. Then please note that normal operation using external resolver input signal becomes invalid while excuting BIST.

■BIST circuit schematic configuration



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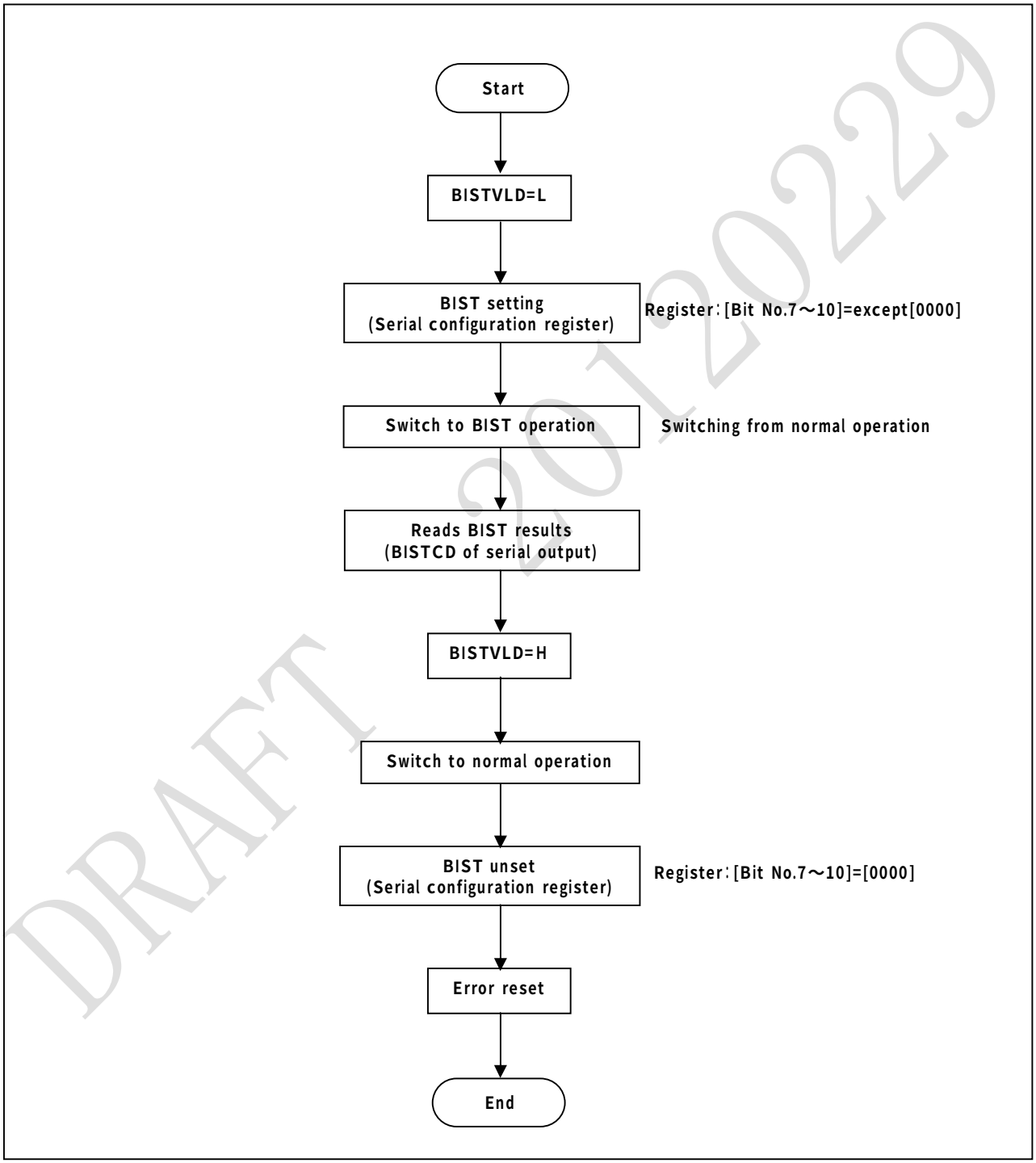
7.2 Execution Method of BIST

BIST function is active when "BISTVLD" input is "Low". And BIST will be excuted while configuration registers (Bit No 7~10) has been set. The result can read by serial output BIST code (BISTCD1~BISTCD4) when BIST is excuting. The following shows the basic execution flow.

■ BIST excution flow

—If you run only a specific set BIST.—



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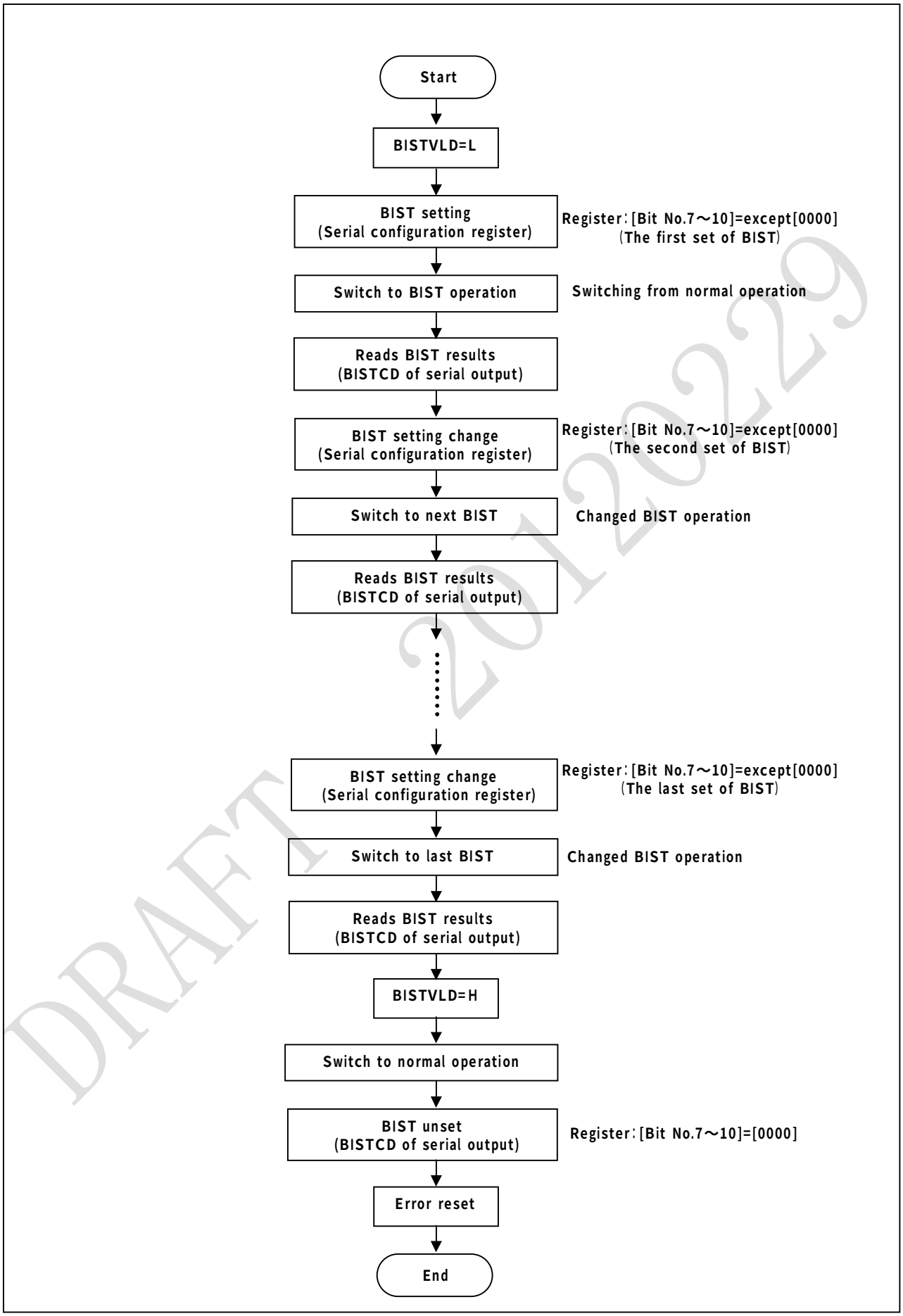
※ The order is not issue for "BISTVLD=L switching" and "BIST setting". The reverse case, switching to BIST operation is getting valid by "BISTVLD=L switching".

※ The order is not issue for "BISTVLD=H switching" and "BIST unset". The reverse case, switching to normal operation is getting valid by "BIST unset".

—If you run multiple consecutive BIST configurations—



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■Considerations for BIST execution

When you perform BIST, please note the following points.

① Must be run with "INHB=High".

② Please set more than 10ms latency for reading BIST result of BIST execution from normal operation, and for reading BIST result of the BIST configuration changes under BIST mode.

③ After any BIST is completed and switch to normal mode, the external filter is reset once.

④ The error reset should be performed after any BIST is completed.

⑤ Please set more than 10ms latency to excute error reset after switching to the normal operation mode from BIST mode.

7.3 Result of BIST

Each BIST result indicate their specific code of BISTCD1~4 which is assigned as Bit3~6 of serial output mode [11](Result of BIST). The diagnosis result that is falling edge timing of SCSB output as serial data.

■Description of BIST results

BIST CD4	BIST CD3	BIST CD2	BIST CD1	Description of BIST results	Remarks
0	0	0	0	(default value)	Except duration of BIST operation
0	0	0	1	—	
0	0	1	0	—	
0	0	1	1	—	
0	1	0	0	—	
0	1	0	1	Matched to the BIST command angle 1 (0 °)	Matching range: ±1.4 ° max
0	1	1	0	Matched to the BIST command angle 2 (45 °)	Matching range: ±1.4 ° max
0	1	1	1	Matched to the BIST command angle 3 (270 °)	Matching range: ±1.4 ° max
1	0	0	0	—	
1	0	0	1	—	
1	0	1	0	Normal operation for broken wire detection BIST (COS signal line)	
1	0	1	1	Normal operation for broken wire detection BIST (SIN signal line)	
1	1	0	0	—	
1	1	0	1	—	
1	1	1	0	—	
1	1	1	1	Abnormal BIST	

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8. Function of Fault Detection

AU6803 (AU6804) has built-in test function of fault detection. These error conditions output at the "ERR" or "ERRHLD" terminal and error code which describe error contents output from the ERRCD1~3 by output setting. The 4 kind of contents of detection are shown below.

- Abnormal Resolver Signal (Square-sum method)
- Break Detection of Resolver Signal Line (DC-bias method)
- Abnormal R/D conversion (PLL Unlock)
- Abnormal High Temperature inside IC

In this chapter, describe each detection method and typical fault detection pattern and also describe corresponding error code, their priorities, and error reset method.

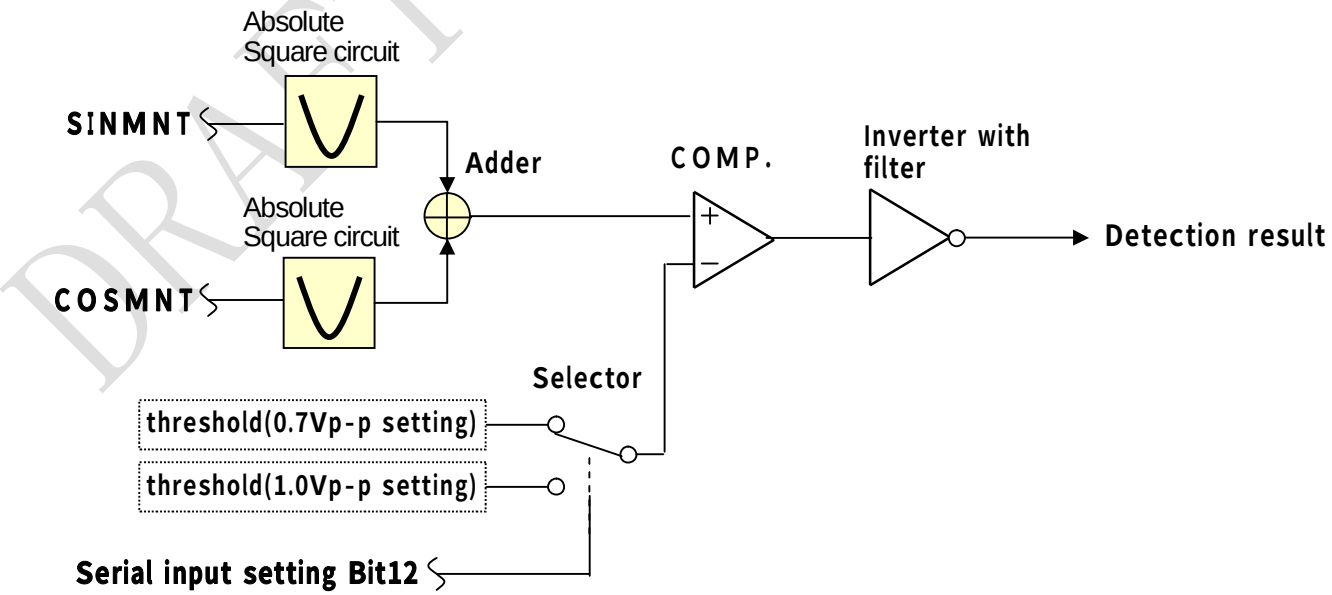
This built-in test function is independent from R/D conversion function and does not restrict any output of R/D conversion IC as a result of this failure. However, when Resolver signal is returned from abnormal resolver signal state or any breaking of line, the external filter(loop filter) is reset once.

8.1 Abnormal Resolver Signal (Square-sum method)

8.1.1 Concept Detection

This concept is to detect fault status that monitor output amplitude balance is disturbed. In case of shorted/breaking-down state of exciting line, resolver is not excited and signal will disappear then this situation can detect as fault status. Also short circuit between signal lines S1-S3, S2-S4), or rear short circuit of resolver winding, etc. may be detected if the state satisfies the abnormality determination.

8.1.2 Circuit Configuration



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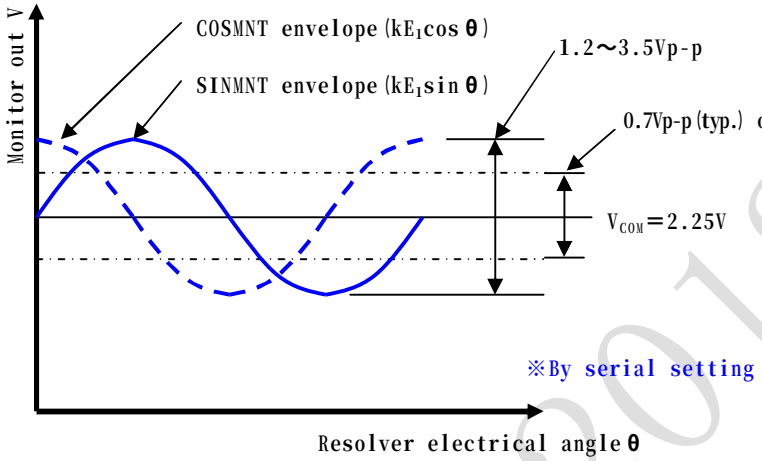
8.1.3 Detection Principle

The detection principle is making comparison between threshold value and absolute square sum value ($\sqrt{|SINMNT|^2+|COSMNT|^2}$) of SINMNT/COSMNT output. If square sum value is getting below the threshold, it is detected as fault status. And this threshold value can be changed by updating of serial input setting register.

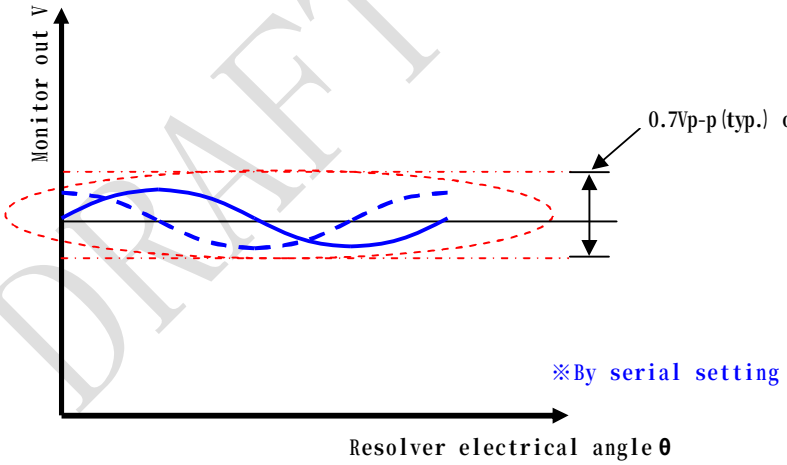
8.1.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal



In normal monitor signal case, absolute square sum value of SINMNT/COSMNT always exceed threshold, then it does not detect as fault.

(2) Detection pattern① (Absolute square sum value of monitor is under threshold)



Breaking/down of exciting circuit or smaller monitor output will detect as abnormal signal in full angular range.

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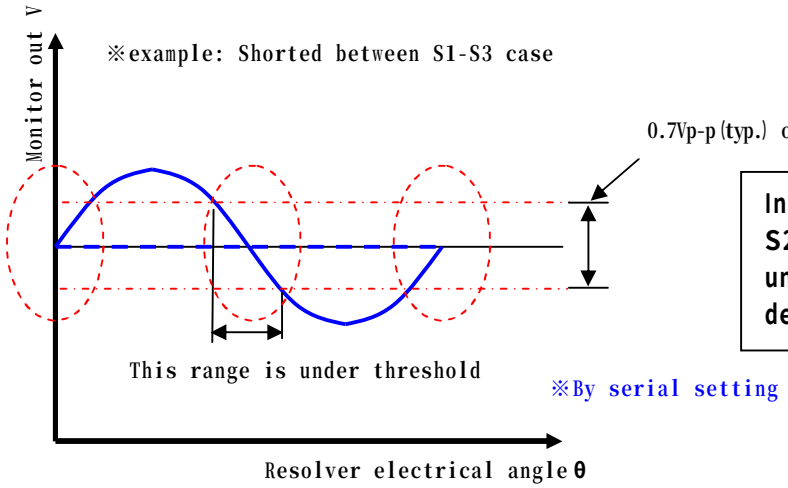
(3) Detection pattern② (Shorted between S1-S3 or S2-S4)



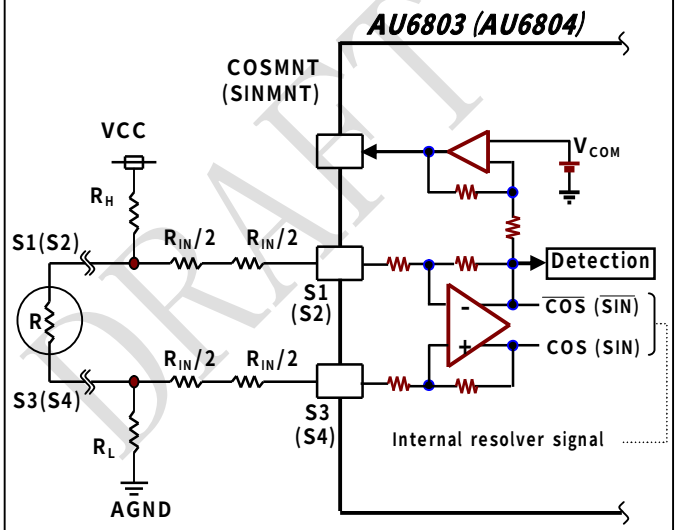
In case of short between S1-S3 or S2-S4, when normal signal amplitude go under the threshold value, error can detect in such angle range.

8.2 Break Detection of Resolver Signal Line (DC-bias method)

8.2.1 Concept Detection

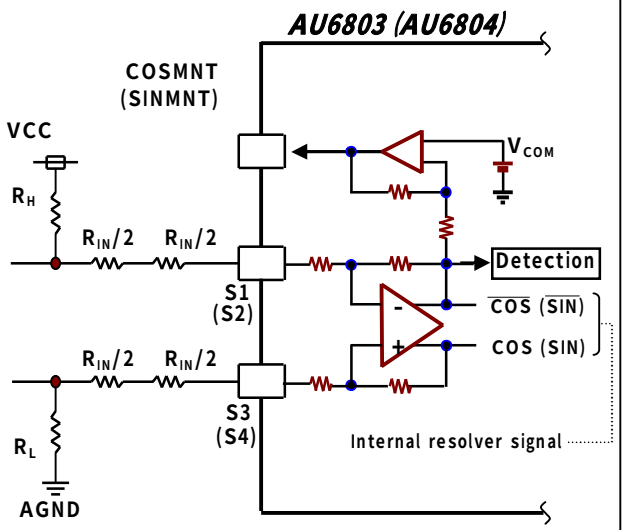
In the resolver signal input circuit, applying the external DC bias circuit(refer 4.2.2) will make the reverse-side DC level of internal resolver signal ($\overline{COS}$ or $\overline{SIN}$) shifted from V_{COM} voltage of reference potential to AGND side when resolver signal line is broken. And monitor output signal shift from V_{COM} voltage to VCC side. Concept detection is to detect this DC level shift of reverse-side of internal resolver signal.

[In DC view:Normal-resolver signal input circuit]



Resolver DC [R] ≪ DC bias [R_{BH} or R_{BL}]. In this case, Resolver terminal S1/S3(or S2/S4) are same potential. Then internal resolver signal (COS or SIN) is getting to be reference potential V_{COM}.
(Monitor output is also V_{COM} level of DC view.)

[In DC view:Breaking-resolver signal input circuit]



Breaking line case, "VCC-AGND" entered to differential amplifier circuit input. Then internal resolver signal (COS or SIN) shift from reference V_{COM} voltage to AGND side.
(Monitor output shift to VCC side.)

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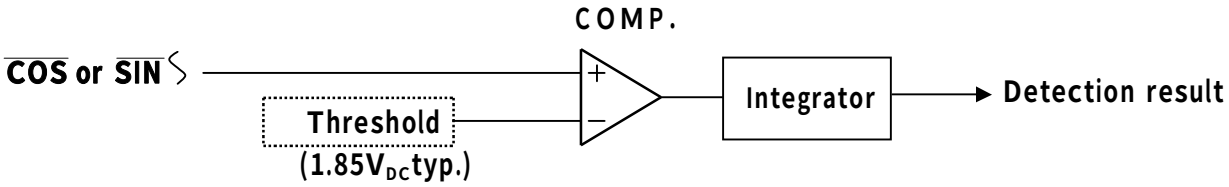
8.2.2 Circuit Configuration



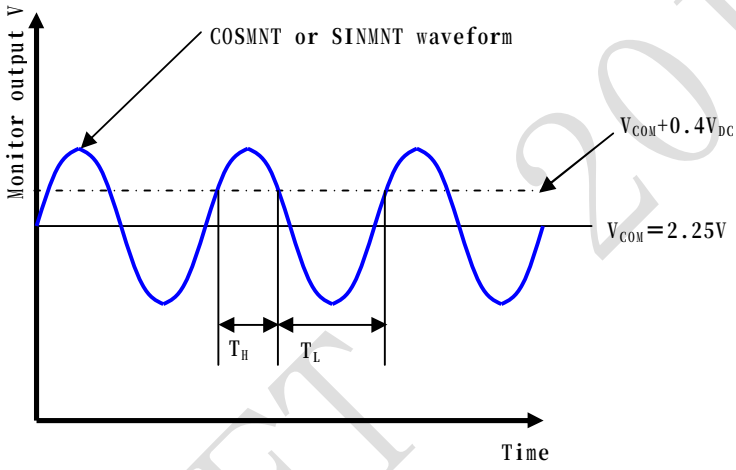
8.2.3 Detection Principl

The principle is comparison between internal resolver signal voltage and threshold. If the time which counts below the threshold is longer than the time(T_L) which exceeds the threshold, it is detected as fault situation.

In monitor output case, if the time (T_H) which exceeds 2.65V_{DC}typ is longer than the time (T_L) which counts below its voltage, it is detected as fault situation.

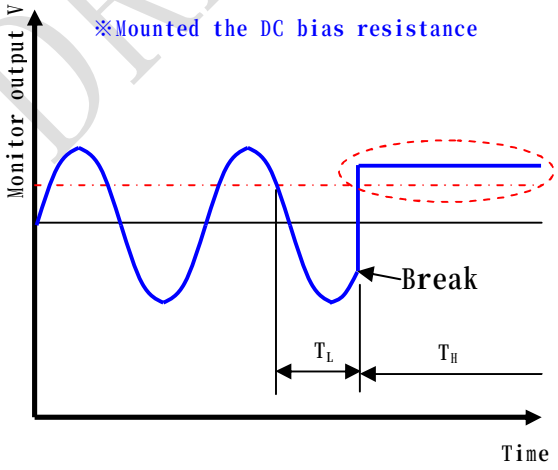
8.2.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal



In normal monitor signal case, both SINMNT and COSMNT show "T_H<T_L" situation then it does not detect as fault.

(2) Detection pattern③ (Breaking between S1-S3 or S2-S4)



In case of breaking signal line, the monitor output DC level will exceed threshold value due to DC bias resistance and this "T_H>T_L" situation can detect as fault.

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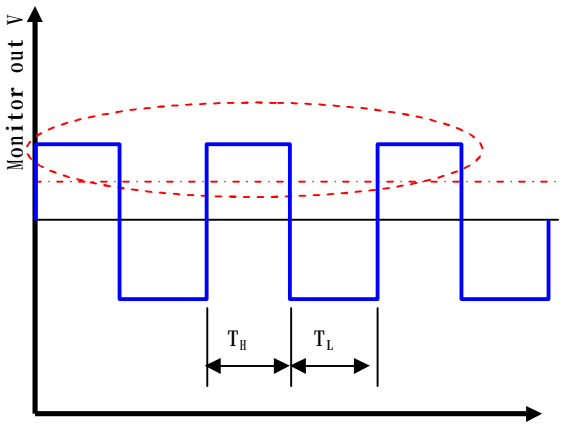
(2) Detection pattern④ (Rectangle monitor output waveform)



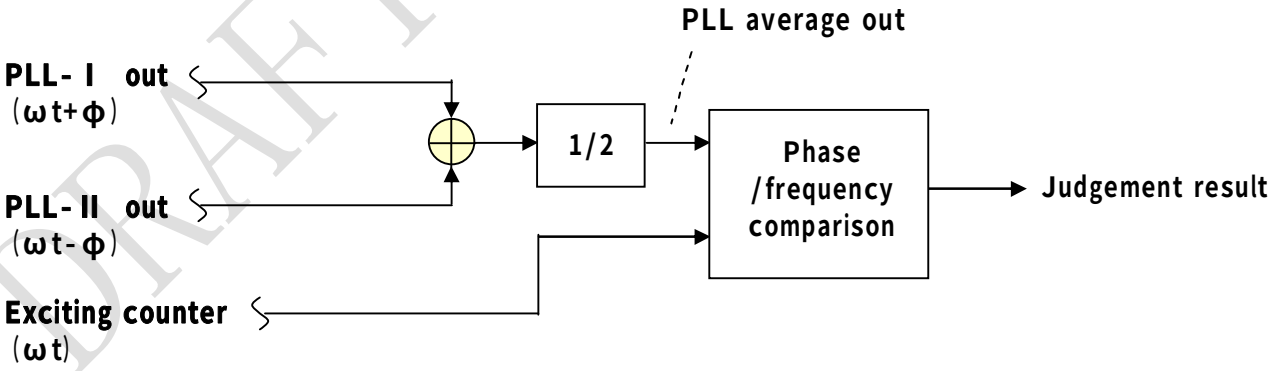
When the monitor output is in a rectangular wave to be saturated, it will be "T_H=T_L" condition then it might be detected as fault situation due to boundary conditions for the determination.

8.3 Abnormal R/D conversion (PLL Unlock)

8.3.1 Concept Detection

Twin-PLL (refer chapter 1.3 or 11.1) which is a R/D conversion method of this product are composed of two PLL. In normal conversion activity, by taking the difference of each PLL output (ωt+φ, ωt-φ), it is possible to obtain digital data corresponding to resolver angle. Also average value of each PLL output becomes to the excitation frequency and maintain the certain relationship between each phase. This concept detection is to detect a state which the average value of the output frequency of each PLL or a state which phase relationship has collapsed. These conditions are defined as state that is not established normal R/D conversion and they are detected as fault situation.

8.3.2 Circuit Configuration



8.3.3 Detection Principl

The principle is to make comparison of phase and frequency between average value※ (counter output) of the two PLL outputs and exciting counter output※ which is the counter output for generating an excitation signal. When the frequency has become a mismatch or phase relationship has collapsed, it is detected as fault.

※ These output signals can not be verified from the outside of this product.

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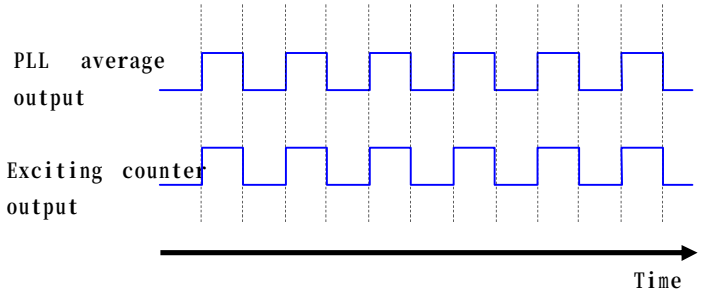
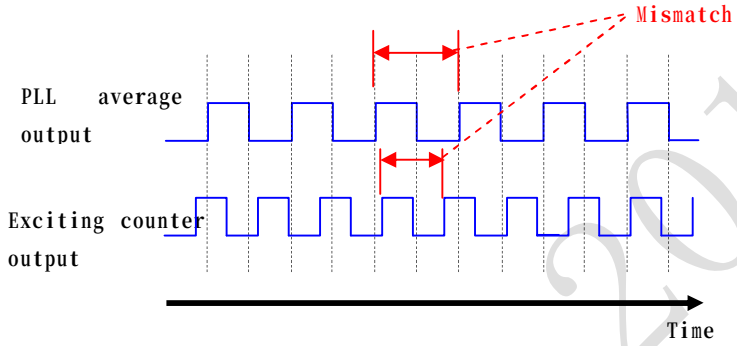
8.3.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal



In normal R/D conversion state, PLL average output value and exciting counter output (frequency) are matched. Also phase maintain a certain relationship. Then it is not detect as fault.

(2) Detection pattern⑤ (PLL unlock)



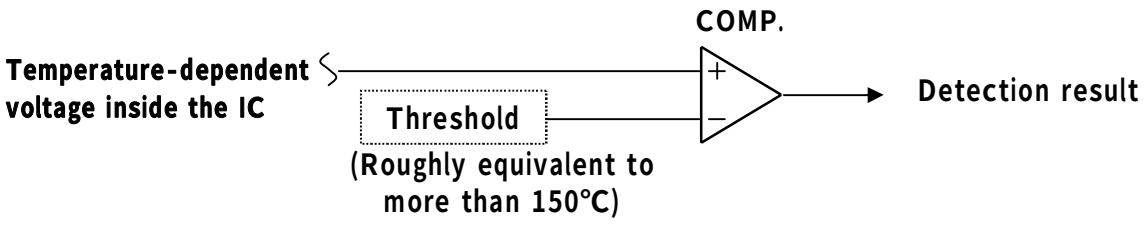
When PLL unlocked and R/D conversion is not performed normal, the phase relationship between PLL average output and exciting counter output has changed and frequency is getting mismatched. Then it is detected as fault situation.

8.4 Abnormal High Temperature inside IC

8.4.1 Concept Detection

In this detection concept, a state which the IC junction temperature exceed 150°C is defined as a state leading to product failure, then it is detected as fault. The product which is detected as this abnormal high temperature might be damaged their circuit by heat even back to the normal state. So please do not use such products.

8.4.2 Circuit Configuration



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8.4.3 Detection Principl

The principle is to make comparison between the generating voltage which characteristic depend on the temperature at the internal and threshold voltage which equivalent to more than 150℃. If it exceeds the threshold temperature it is detected as fault.

8.4.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal

If device usage is inside of specified operating temperature (ambient temperature), power derating, and voltage, it is not detected as fault as long as the product is not defective.

(2) Detection pattern⑥ (outside condition usage against specified)

There might be possibility to detect as fault in below state, loss exceeds the allowable state or ambient temperatures above 125℃, load larger than the specified connection or larger than the specified voltage, in the situation raises heat departing from the specification.

(3) Detection pattern⑦ (IC Corruption)

If there is a situation such as excessive current flows through the internal IC due to some failure, it might be detected as fault.

8.5 Fault Detection Contents and Error Code

Error code was assigned for each fault. When fault is detected, error state output from "ERR"and "ERRHLD" terminals and ERRC1~3 will be output from the contents detected as an error code. In case of simultaneous errors, only the error code with priority is indicated.

■Error code (Result of failure detection) list

ERR CD3	ERR CD2	ERR CD1	Description of Error (Result of failure detection)	Priority ※	Remarks
0	0	0	No abnormal state	—	No error output
0	0	1	Abnormal resolver signal (square sum)	3	
0	1	0	Broken wire of resolver signal (COS line)	1	
0	1	1	Broken wire of resolver signal (SIN line)	2	
1	0	0	Abnormal R/D conversion (PLL unlock)	4	Out of Freq lock
1	0	1	(Not defined)	—	
1	1	0	Abnormal high temperature inside IC (approxmately 150℃ or more)	5	
1	1	1	Error mask when starting (After releasing reset)	—	

※ Smaller numbers are getting higher priority.

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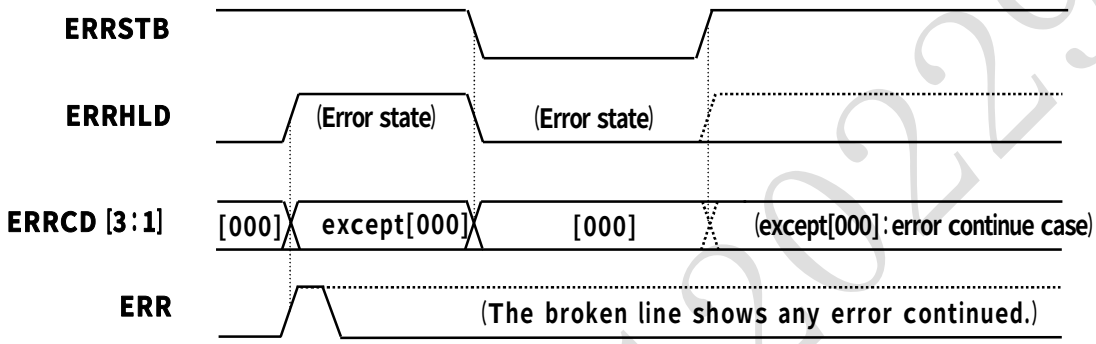
8.6 Error Reset

The contents of “ERRHLD” and error code (ERRCD1~3) which is set by detecting fault is reset by setting”ERRSTB=Low”.

■Error-reset operation waveform



※ For timing detail, please refer 10.9 .

※ The ERRHLD output should be used after the error is reset by the ERRSTB input. When the ERRHLD output can not be released by the Error Reset, remove the true cause of error referring to the section 9.1.

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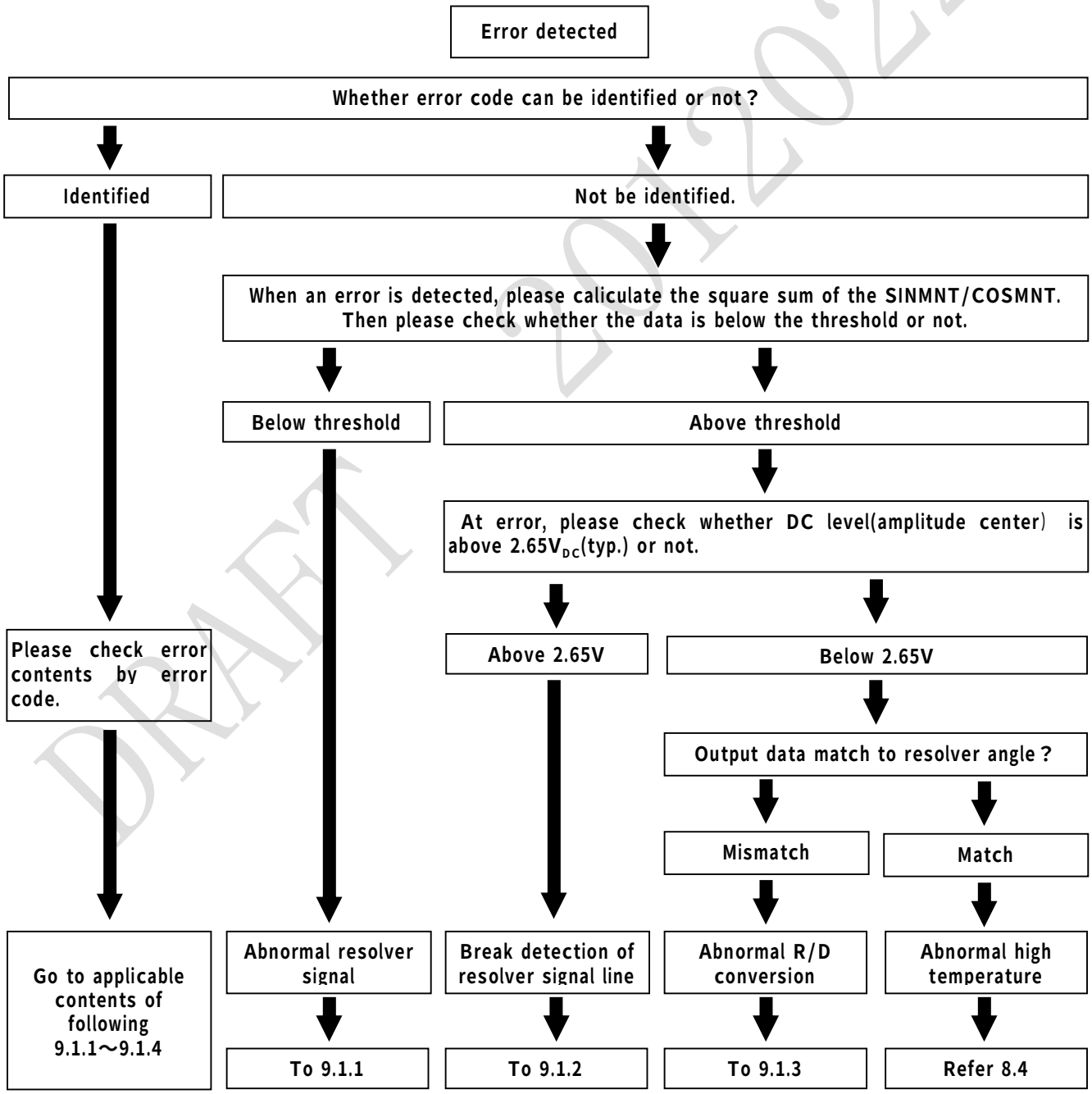
9. If you think trouble shooting

In this chapter, there are corresponding examples for the case of error detected by the function of fault detection, and for the case of strange angle output data. Please check these examples for your troubleshooting and operation check.

9.1 In case of error detection

When an error is detected (ERR or ERRHLD output are "H" level), refer to the following troubleshooting flow. Firstly please perform to estimate reason of fault detection, and error factor should be identified and eliminated according to the procedure of chapter 8.1.1 or lator. Regarding the operation of fault detection function, please refer chapter 7.

■Troubleshooting flow of error



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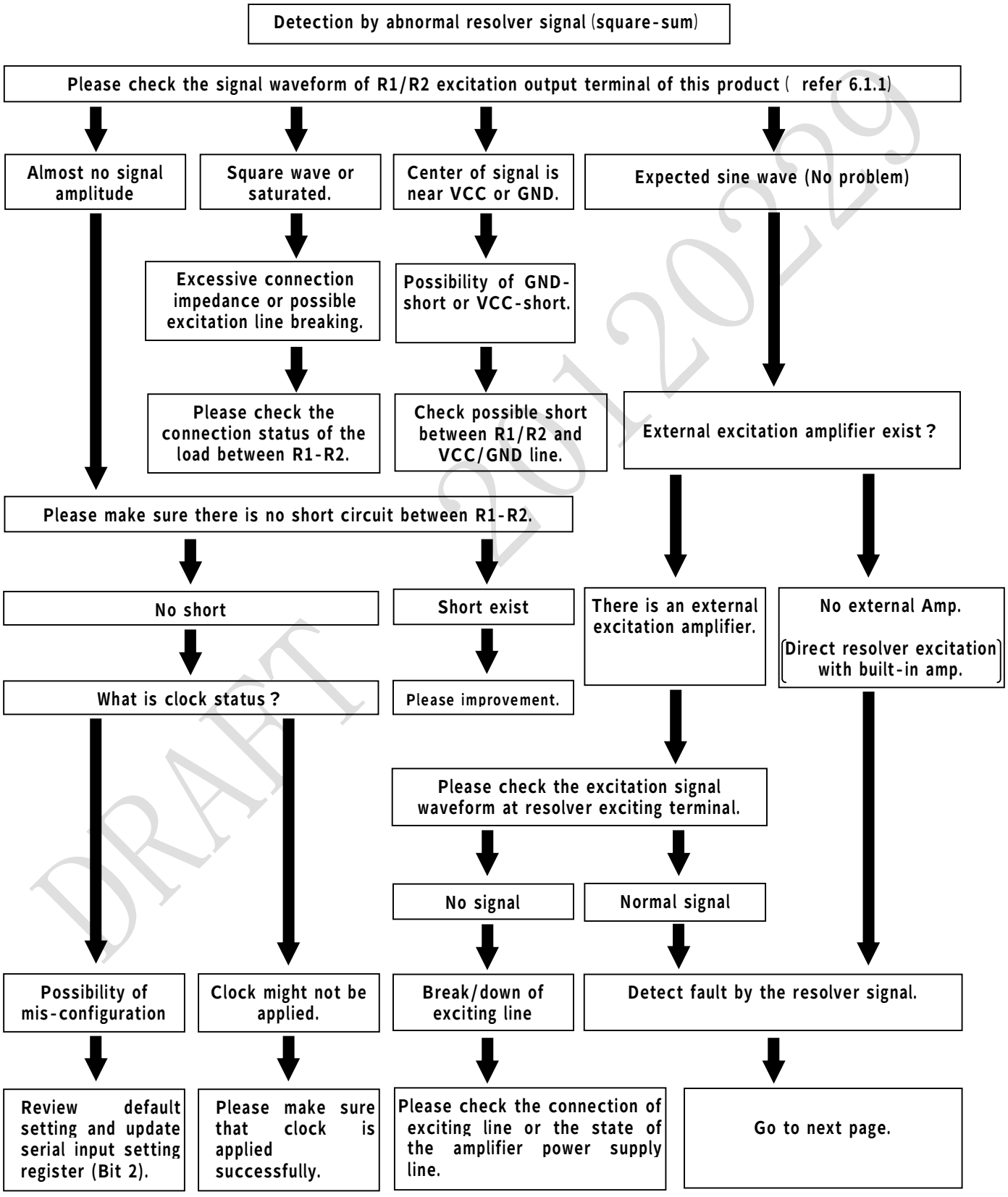
9.1.1 Suspicion of Abnormal Resolver Signal (Square-sum method)

In case of suspicion of abnormal resolver signal (square-sum method) detection, true error factor should be identified and eliminated according to the below troubleshooting flow.

■Troubleshooting flow of abnormal resolver signal



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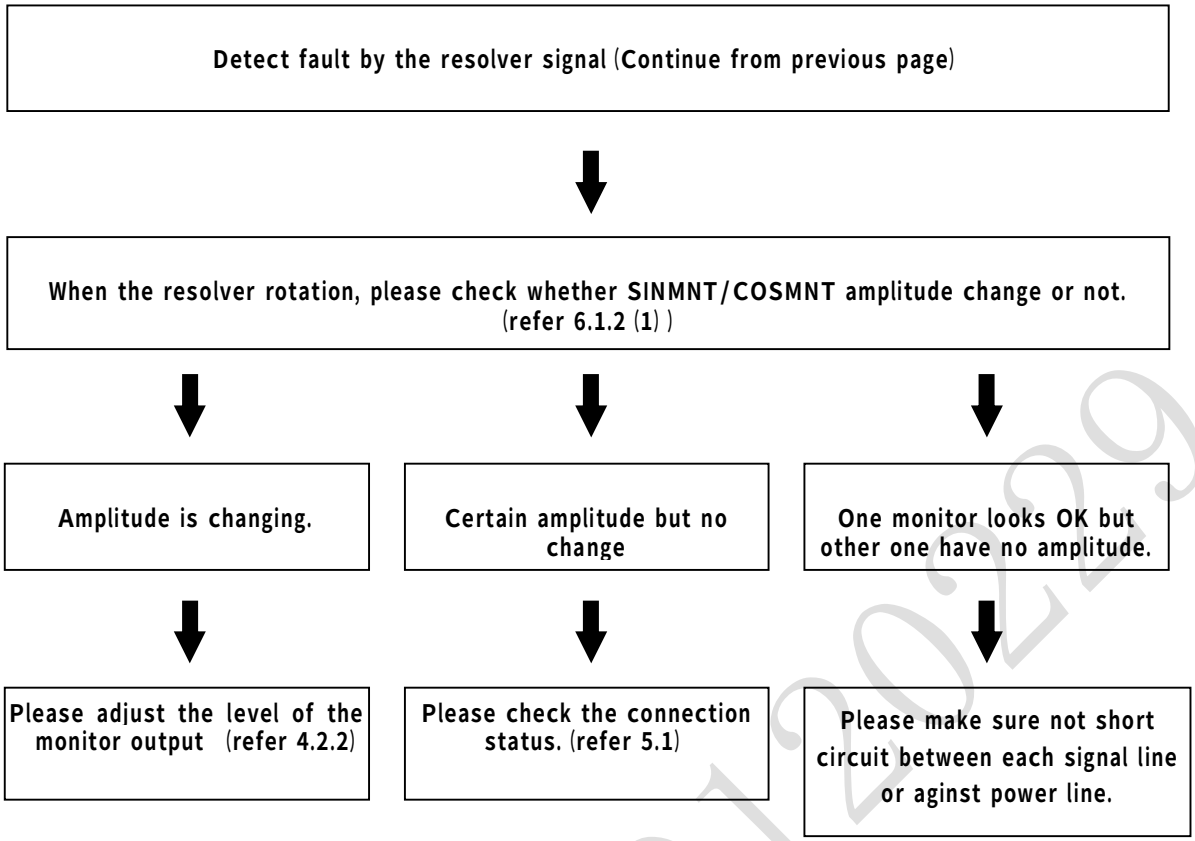

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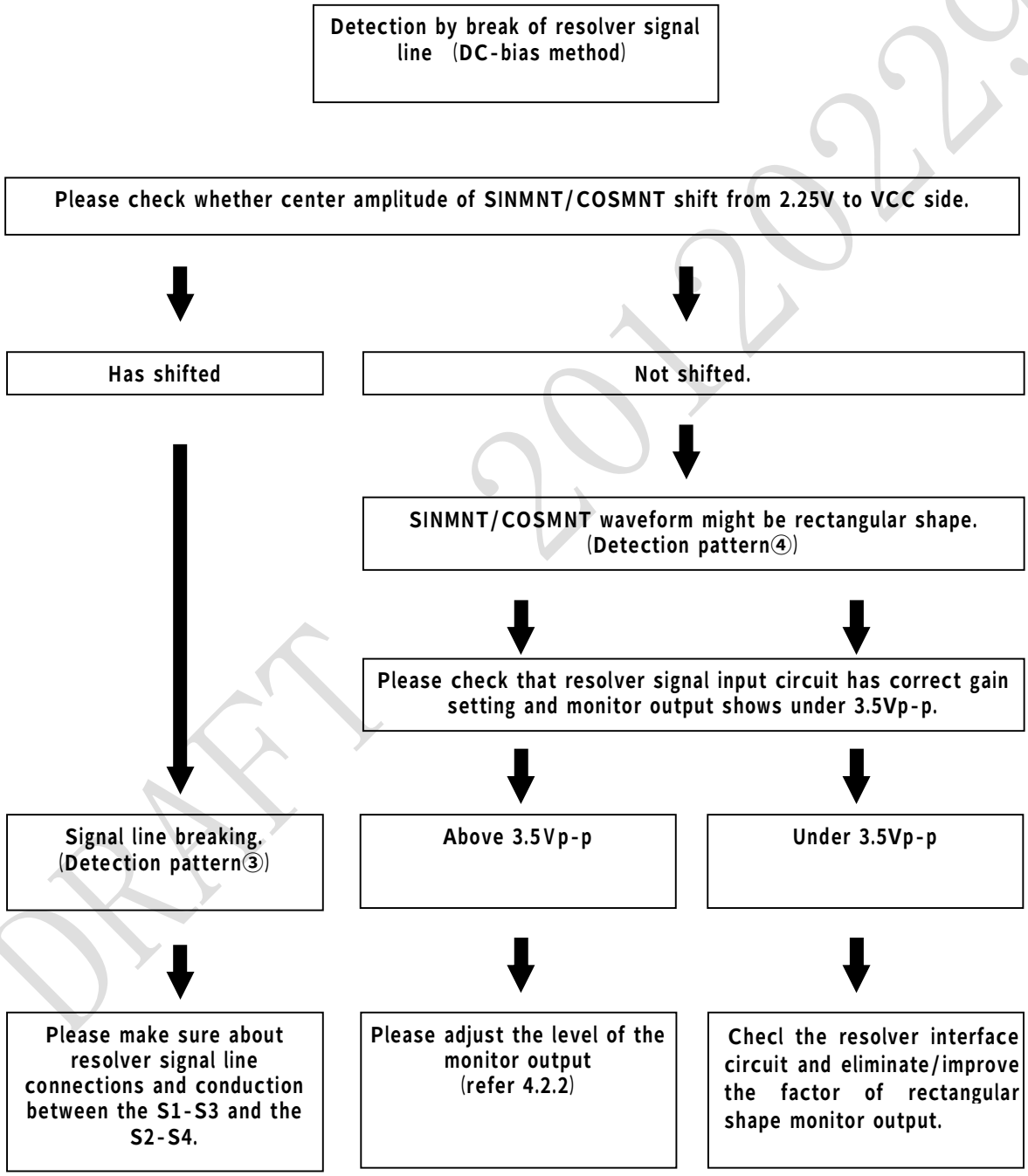
9.1.2 Suspicion of Break Detection (DC-bias method)

In case of suspicion of break detection of resolver signal line (DC-bias method), true error factor should be identified and eliminated according to the below troubleshooting flow.

■Troubleshooting flow of detecting break of resolver signal line.



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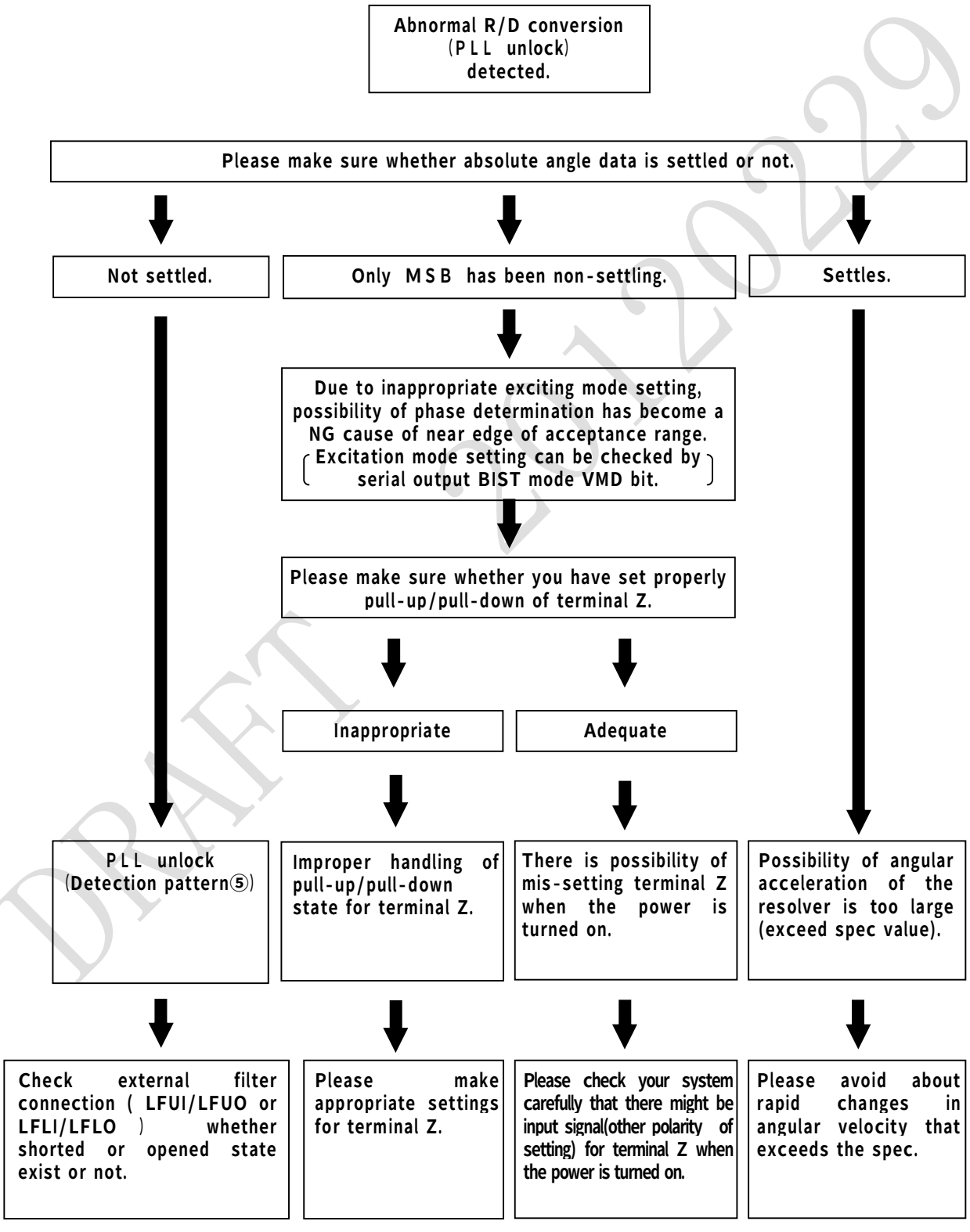
9.1.3 Suspicion of Abnormal R/D conversion (PLL Unlock)

In case of suspicion of abnormal R/D conversion (PLL unlock), true error factor should be identified and eliminated according to the below troubleshooting flow.

■Troubleshooting flow for abnormal R/D conversion detection



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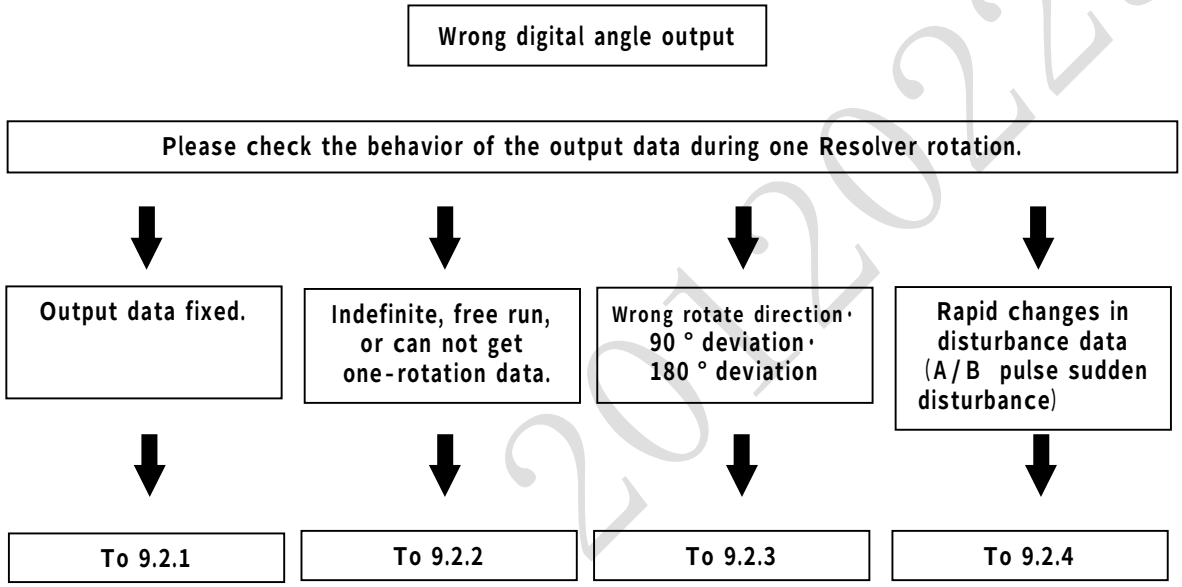
9.2 In case of wrong angle data

Despite the rotating Resolver, angle output data is not changed, or output shows the different format data, or output data is not fit to actual angle. In such case, please follow below troubleshooting flow and identify the behavior of the output data. Then please improve this error condition by the procedure described in chapter 9.2.1 and later.

■Troubleshooting flow of wrong digital angle data.



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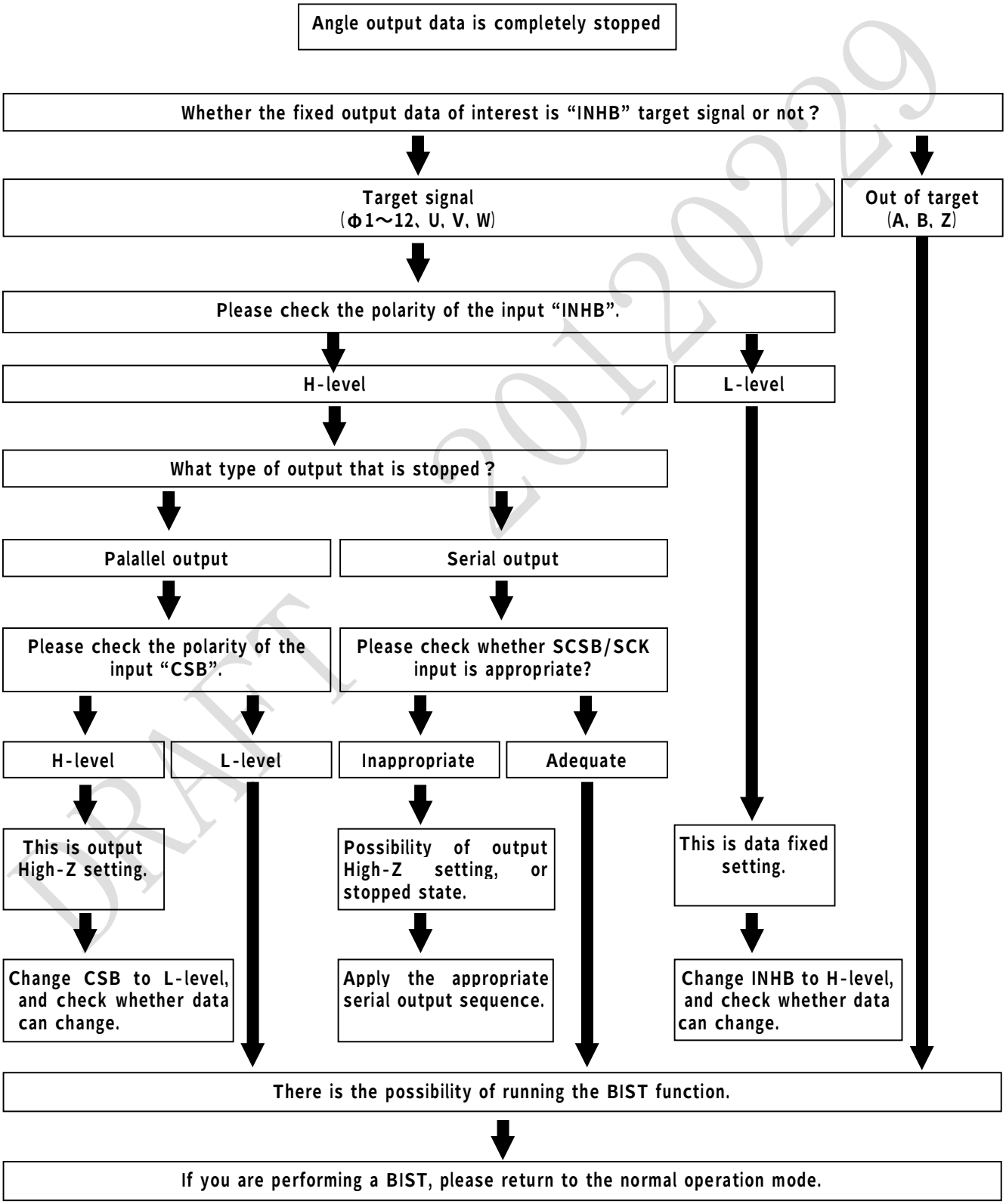
9.2.1 In case of fixed angle data

In case of angle output data is completely stopped, please follow below troubleshooting flow and identify the factors, and then improve your system.

■Troubleshooting flow of fixed angle data



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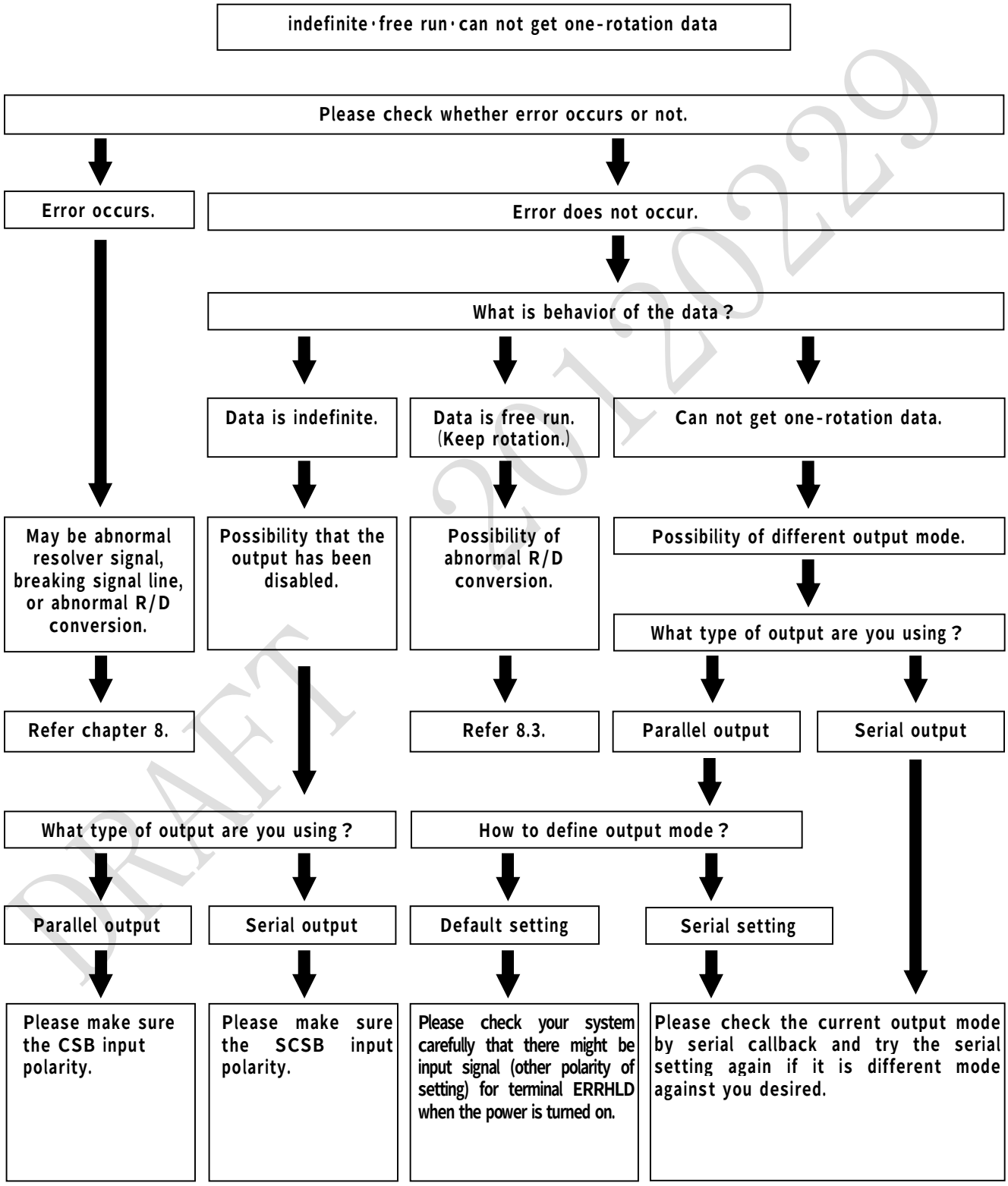
9.2.2 In case of indefinite, free run, can not get one-rotation data

In case of angle output data is indefinite, free run, can not get one-rotaion data, please follow below troubleshooting flow and identify the factors, and then improve your system.

■Troubleshooting flow of indefinite, free run, can not get one-rotation data



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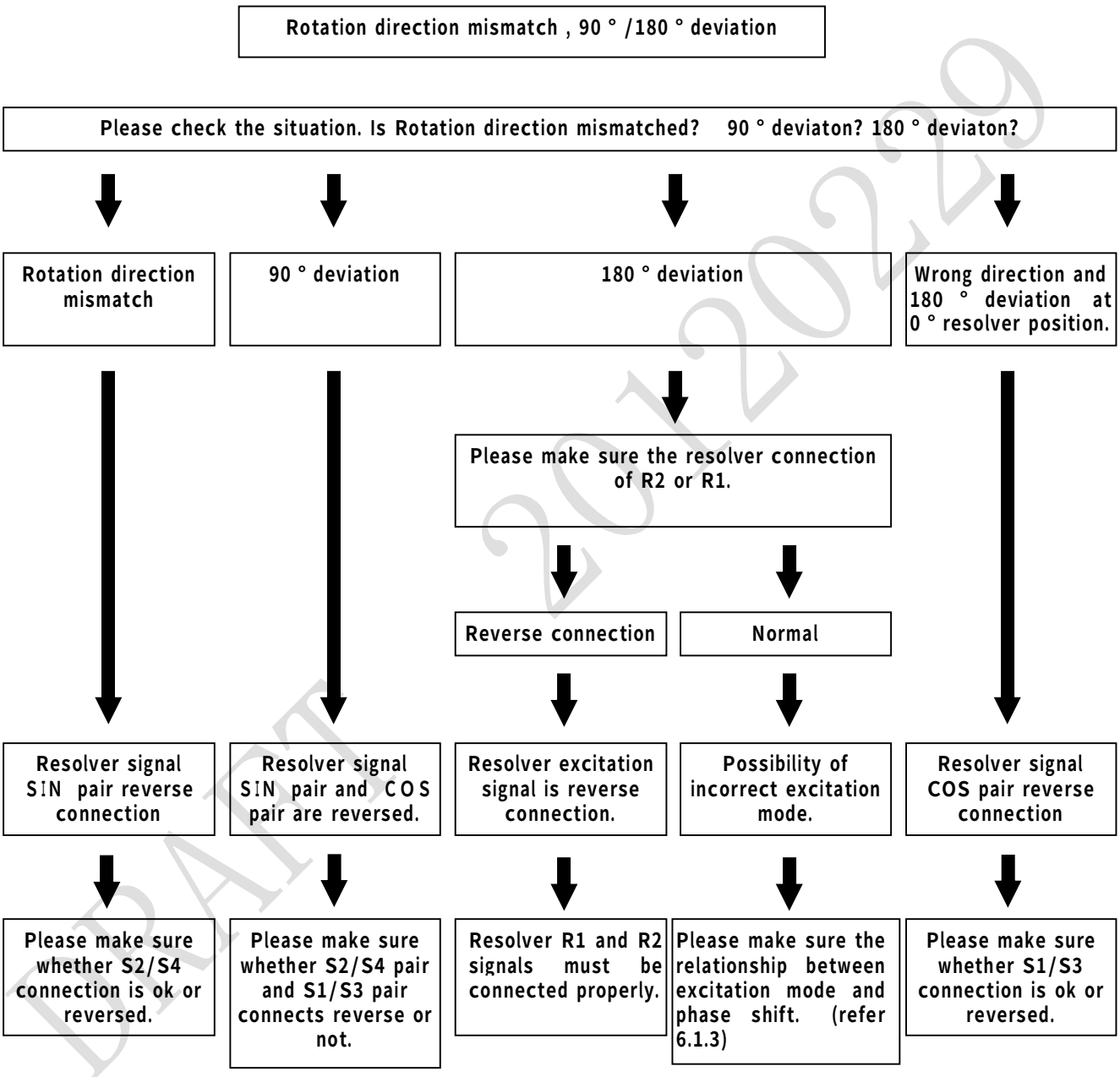
9.2.3 In case of rotation direction difference, 90 ° deviation or 180 ° deviation

In case of angle output data shows rotation direction difference, 90 ° deviation or 180 ° deviation, please follow below troubleshooting flow and identify the factors, and then improve your system.

■Troubleshooting flow of rotation direction mismatch, 90 ° /180 ° deviation



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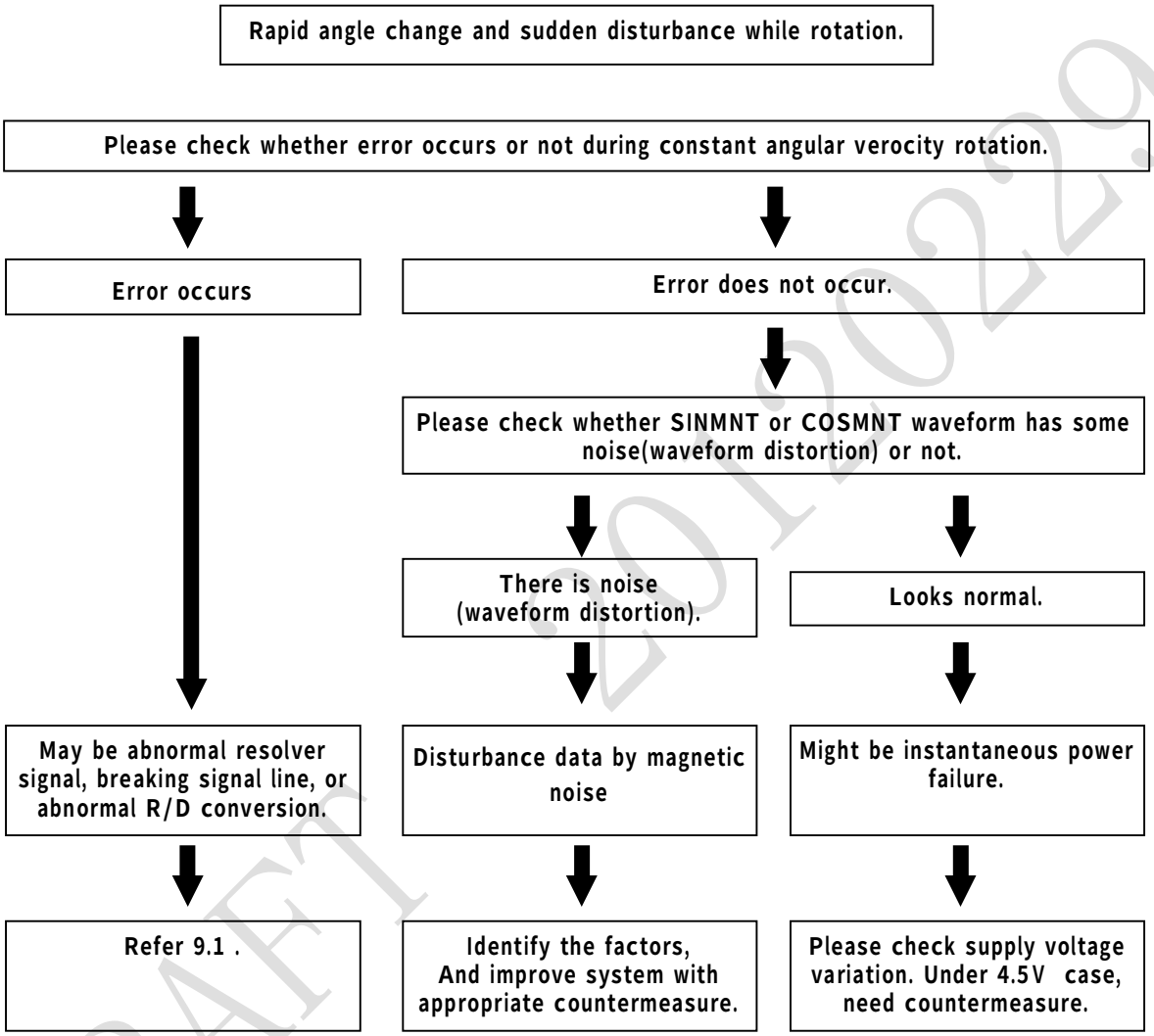
9.2.4 In case of rapid change in the output angle data and disturbance

In case of rapid change in the output angle data or a sudden disturbance while rotation, please follow below troubleshooting flow and identify the factors, and then improve your system.

■Troubleshooting flow of rapid change in the output angle data and disturbance



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9.3 If the situation does not improve

If the situation does not improve even if section 9.1 or 9.2 steps perform, and if there is another phenomenon which does not mention in this manual, please contact us with waveforms when an error occur (appropriate abnormal signal, SINMNT, COSMNT) and also inform us about detail troubled circuit information.

10. Electrical characteristics

10.1 Absolute maximum rating

Items	Symbol	Absolute maximum rating	Unit
Power supply voltage	VCC	-0.3～+7.0	V
	VRR	-0.3～+7.0	V
	VDD	-0.3～+7.0	V
Analog input voltage	V_{Ia}	-0.3～VCC (VRR) +0.3	V
Digital input voltage	V_I	-0.3～VDD+0.3	V
Digital output current	I_O	-10～+10	mA
Operating temperature	T_{opr}	-40～+125	°C
Storage temperature	T_{stg}	-65～+150	°C
Allowable loss	P_D	500	mW

※ If you use the IC beyond the absolute maximum rating, it may cause permanent damage to the IC.

10.2 Power-related characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Power supply voltage	VCC	4.5	5.0	5.5	V	Recommended power supply voltage. VCC, VRR, VDD must be used at the same potential.
	VRR	4.5	5.0	5.5	V	
	VDD	4.5	5.0	5.5	V	
Reset release voltage	Vrsth	3.9	-	4.4	V	Power-On-Reset release voltage
Reset voltage	Vrstl	3.7	-	4.2	V	Power-On-reset voltage
Reset voltage hysteresis	Vrhys	-	0.2	-	V	Vrsth-Vrstl
Supply current	$I_{CC}1$	-	-	45	mA	CSB=H/Supply current at static angle※
	$I_{CC}2$	-	-	50	mA	CSB=H/Maximum rotation or CSB=L/supply current at static angle※
	$I_{CC}3$	-	-	60	mA	CSB=L/Supply current at maximum rotation※

※ Internal current consumption of the digital output at no load, include exciting current.

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10.3 R/D conversion characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Resolution			12		Bit	A number of divisions per electrical angle.
Conversion accuracy		-4	-	4	LSB	Absolute error of the electrical angle input in a stationary state.
Repeatability		-2	-	2	LSB	Repeatable angle accuracy
Settling time			1.5		ms	Input step of 180 ° electrical angle Settling range：±8LSB max.
Maximum angular velocity 1		240,000			min^{-1}	10MHz ＜ Ext-CLK ≦ 12MHz Angular velocity range capable of tracking in the electrical angle.
Maximum angular velocity 2		180,000			min^{-1}	8MHz ＜ Ext-CLK ≦ 10MHz、or internal clk operation mode. Angular velocity range capable of tracking in the electrical angle.
Maximum angular acceleration		1,000,000			rad/s^2	Angular acceleration range capable of following.
Responsibility		-0.2		0.2	deg./ 10,000min^{-1}	Output response delay in a constant angle velocity. (Equivalent to 3.3μs)
Stabilizing time at start				20	ms	Stabilizing time of output at start. (±8LSB max at static state)

10.4 Built-In Self-Test (BIST) characteristic

items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
R/D conversion BIST (0 ° /45 ° /270 °)						
Determination threshold		-1.4	-	1.4	deg.	Allowable range for the setting angle.
Determination time		-	-	10	ms	The time required to stabilize BIST results.
Failure detection BIST (Broken wire BIST)						
Determination time		-	-	10	ms	The time required to stabilize BIST results.

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10.5 Failure detection characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Abnormal resolver signal (Square sum method)						
Detection threshold 1		0.5	0.7	0.9	Vp-p	Setting register Bit12 = 0 case. The other voltage amplitude when any one of monitor output is 0V.
Detection threshold 2		0.8	1.0	1.2	Vp-p	Setting register Bit12 = 1 case. The other voltage amplitude when any one of monitor output is 0V.
Relative deviation between range		0.2	0.3	0.4	Vp-p	Threshold_2 – Threshold_1
Determination time		-	-	2	ms	Time required detecting fault.
Broken wire of resolver signal (DC bias method)						
Detection threshold		0.33	0.4	0.5	V	DC level variation of monitor output voltage.
Determination time		-	-	10	ms	Time required detecting fault.

※ In case of the continuous time of failure is shorter than above detection time, there is possibility not to detect failure.

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10.6 Analog signal characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Excitation output						
Output current		8.08	9.5	10.92	mArms.	
Output frequency 1		8	10	12	kHz	Frequency range when using the internal clock
Output frequency 2			f_{CLK}/ 1024		Hz	Frequency by external clock. (f_{CLK}= external clock frequency)
Load impedance				200	Ω	Allowable load impedance of R1/R2.
Resolver signal input						
Input protection resistor		-	180	-	Ω	
Input amplifier feedback resistor	R_F	37.8	41.5	45.2	kΩ	
Relative accuracy of above resistor		-1	-	1	%	
Career gain		-20	-	20	%	The variation of monitor output voltage when resolver is directly excited by the R1/R2 of this IC.*
Resolve signal monitor output						
Internal reference voltage	V_{COM}		2.25		V	SINMNT, COSMNT terminal center voltage.
Max output amplitude		3.5	-	-	Vp-p	
Load impedance		20	-	-	kΩ	Allowable load impedance of SINMNT and COSMNT.
Velocity output						
Signal value 1		7	10	12	$\mu V/min^{-1}$	Setting register Bit11 = 0 .
Signal value 1 Temperature cofficient		-	0.025	-	$(\mu V/min^{-1})$ /°C	
Signal vlue 2		70	100	120	$\mu V/min^{-1}$	Setting register Bit11 =1 .
Signal value 2 Temperature cofficient		-	0.25	-	$(\mu V/min^{-1})$ /°C	
Max output voltage range		3	-	-	V	VELP-VELN differential output voltage
Output voltage offset 1		-0.2	-	0.2	V	Setting register Bit11 = 0.
Output voltage offset 2		-2	-	2	V	Setting register Bit11 =1.
Load impedance		20	-	-	kΩ	Allowable load impedance of VELP and VELN

※ Except the tolerance of input resistances and the performance of resolver itself.

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10.7 DC characteristics of digital signal

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
High level input voltage	V_{IH}	2.0	-	VDD	V	Recommended input "H" voltage for all digital input terminals.
Low level input voltage	V_{IL}	0	-	0.8	V	Recommended input "L" voltage for all digital input terminals.
Input hysteresis voltage	V_H	-	0.2	-	V	
Input pull-up resistance 1	R_{PU}	30	50	85	kΩ	Pull-up resistor value of digital input terminal. (※Applicable terminals BISTVLD, CLKIN, SSDT, SSCS, SCSB, SCK, INHB, ERRSTB, CSB)
Input pull-up resistance 2	R_{PUBI}	72	120	200	kΩ	Pull-up resistor value of digital input terminal. (※Applicable terminals ERRHLD, ERR, Z)
Input leakage current	I_L	-	-	-200	μA	V_I＝DGND。
High level output voltage	V_{OH}	VDD-0.1	-	-	V	I_{OH}＝0mA。
		VDD-0.5	-	-	V	I_{OH}＝-4mA。
Low level output voltage	V_{OL}	-	-	0.1	V	I_{OL}＝0mA。
		-	-	0.5	V	I_{OL}＝8mA。

10.8 AC characteristics of digital signal

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
External CLK input frequency	F_{CLK}	8	10	12	MHz	
External CLK duty	D_{CLK}	40	-	60	%	
Serial CLK input frequency	F_{SCK}	-	-	5	MHz	
Input rise-up time	tri	0	-	1.0	ms	
Input fall-down time	tfi	0	-	1.0	ms	
Output rise-up time	tr	-	4.2	7.3	ns	C_L=15pF。
Output fall-down time	tf	-	2.5	4.5	ns	C_L=15pF。
Transmission delay time (Input buffer)	tpd	-	5.3	9	ns	
Transmission delay time (Output buffer)	tpd	-	4.7	9	ns	C_L=15pF。

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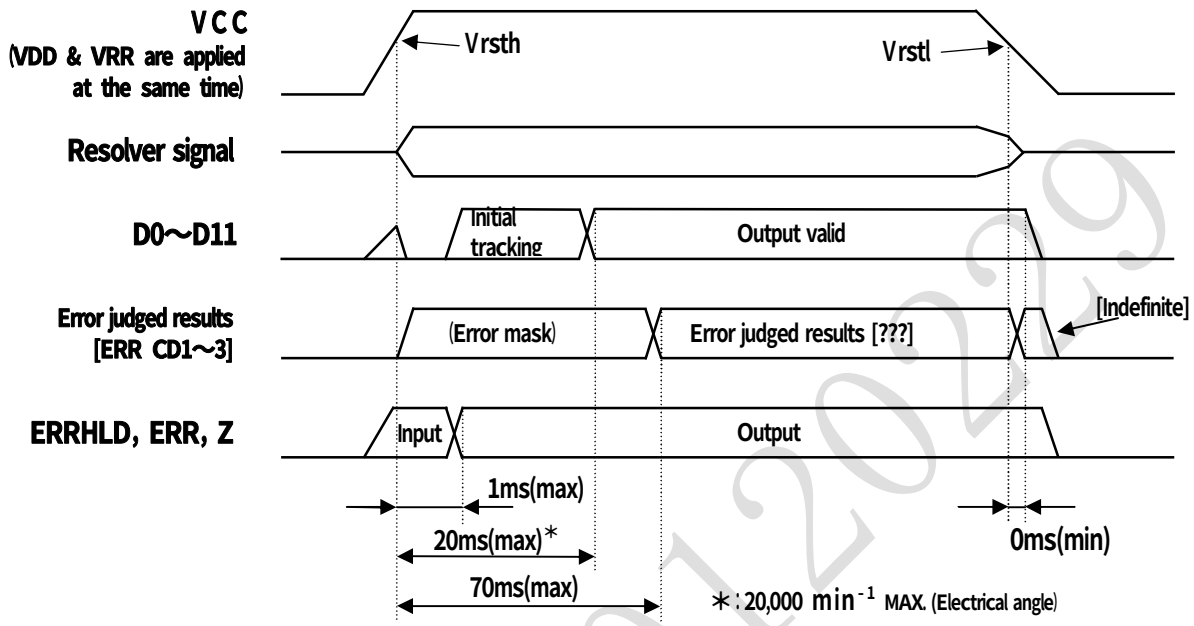
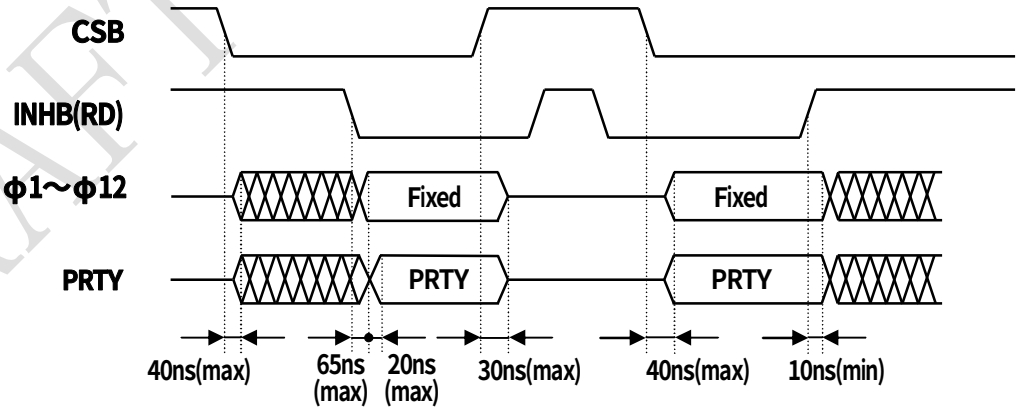
10.9 Timing diagram

■ ON/OFF power sequence



■ Timing of Bus Control



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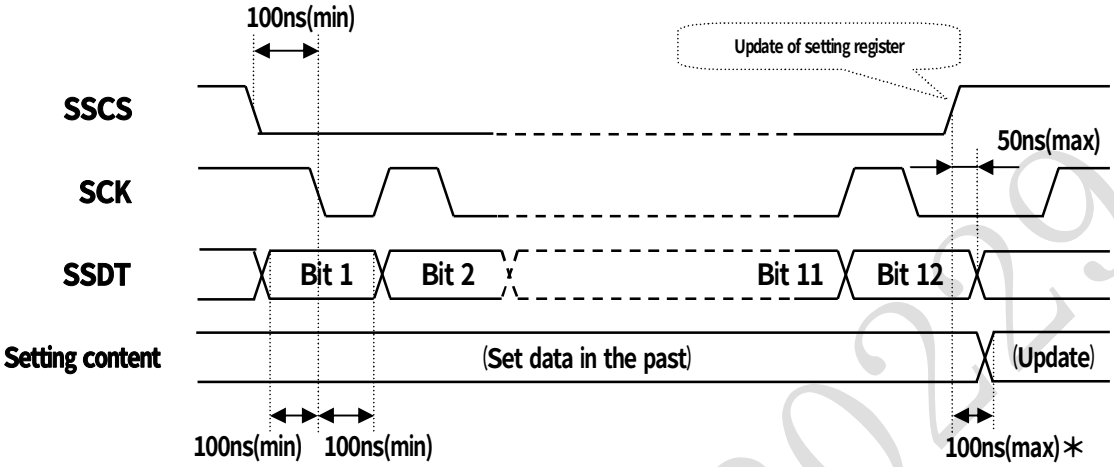
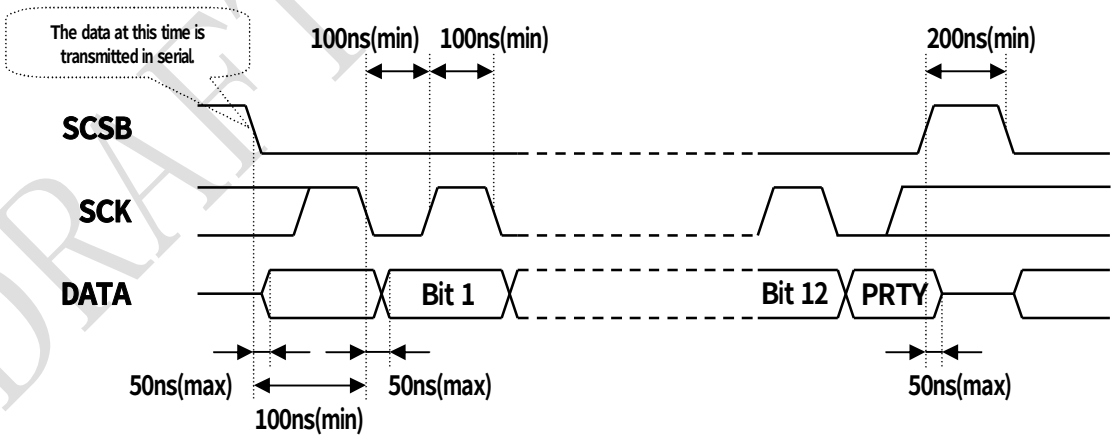
■ Serial input setting sequence



＊: Changing to absolute output mode is exception case.
Please refer section 4.3.2(2) P34 sequence.

■ Waveform of serial output



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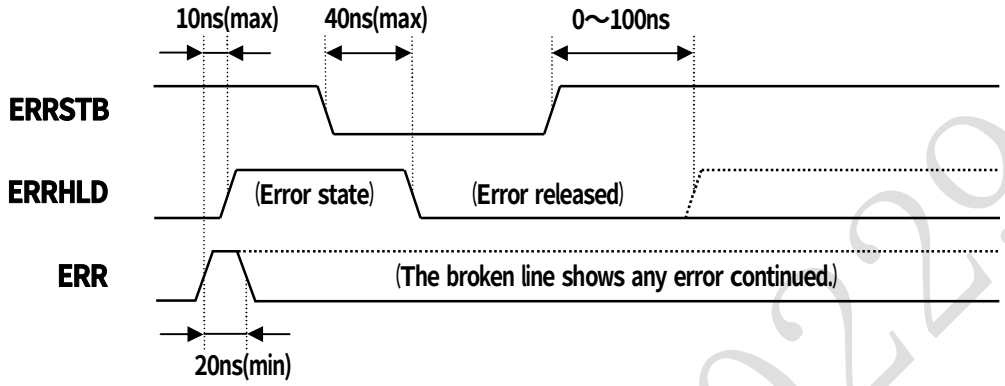
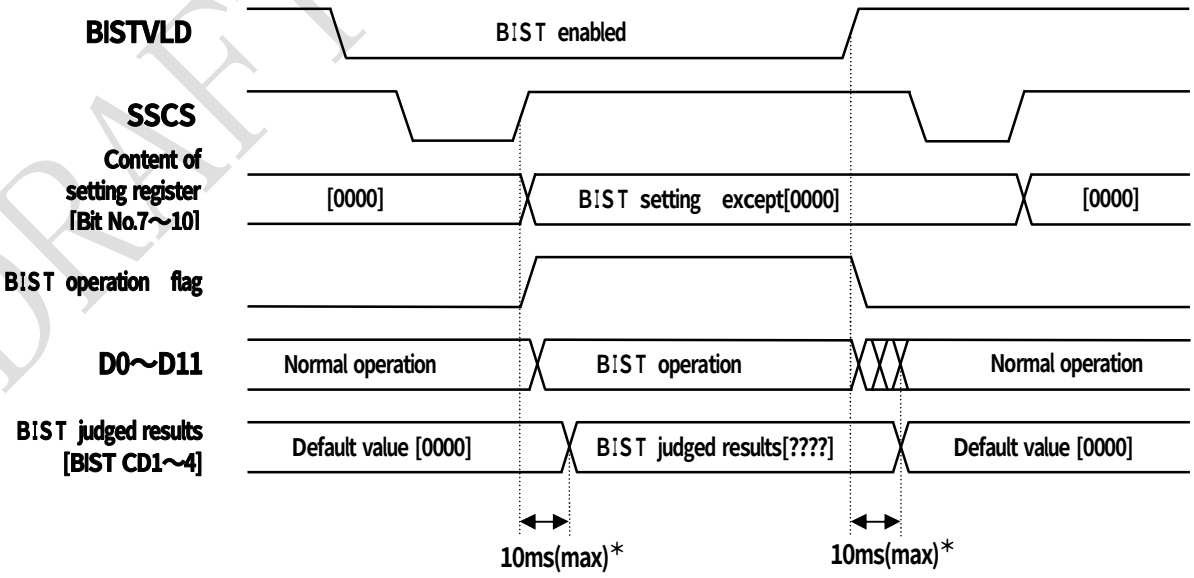
■ Timing of Error Reset



■ Operating sequence of Built-in Self-test (BIST)



*：Only at stationary state

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11. Appendix

11.1 R/D conversion principle

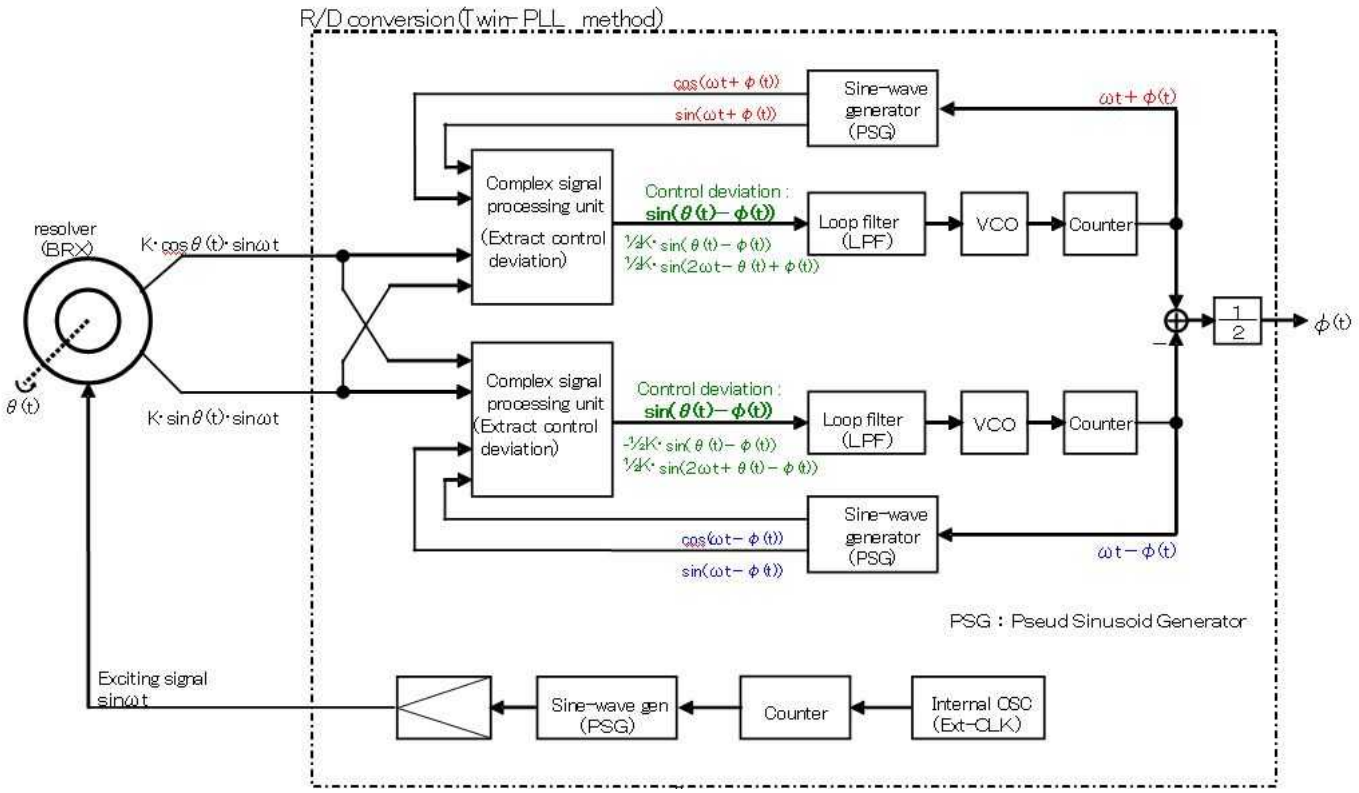
This product adopted Twin-PLL method as R/D conversion system, and it has been configured by two PLL(Phase Locked Loop) configuration and a subtractor to obtain the relative phase angle between the PLL output. Each PLL takes one of the negative feedback controls of closed-loop configuration. A control deviation (ε) is shown in below equation, and it must be controlled as normally "0".

$$\text{Control deviation} \ : \ \varepsilon = \sin(\theta - \phi) \cdot \sin\omega t$$

Here assuming "$\varepsilon = 0$" means "$\theta = \phi$", then resolver analog angular signal can be converted to digital phase angle of PLL output.

One PLL a proceeding phase angle of the output matches the analog resolver angle, and the other PLL a delaying phase angle of the output matches the analog resolver angle. Then output angle "ϕ" can be obtained by calculating the relative phase angle of the two PLL output, and analog angle information can be converted to digital.

■Configuration of Twin-PLL method R/D converter.



[Explanation of concept]

An amplitude modulated resolver signals can think to be composed by signal components of 2 frequency.

$$\text{Sin phase} \ : \ \sin\theta \cdot \sin\omega t = -\frac{1}{2}\cos(\omega t + \theta) + \frac{1}{2}\cos(\omega t - \theta)$$

$$\text{Cos phase} \ : \ \cos\theta \cdot \sin\omega t = \frac{1}{2}\sin(\omega t + \theta) + \frac{1}{2}\sin(\omega t - \theta)$$

In this R/D conversion of Twin-PLL method, One PLL follow the (ωt+θ) frequency component and the other PLL follow the (ωt-θ) frequency component.

An amplitude modulated resolver signals are input to the R/D converter, and each PLL generate control deviation (ε) which is subtracted after multiplied between input signal and sine or cosine signal that is fed back from the output signal of each PLLs. The control deviation (ε) is introduced into the VCO (Voltage Controlled Oscillator) through the compensator that stabilizes the negative feedback loop and improves its performance. The VCO generates the pulse frequency output in proportion to the input voltage and is applied to the counter after it converts from analog to digital. Then we can get (ωt+θ) frequency PLL output and (ωt-θ) frequency PLL output as digital value. These two PLL output has a positive and negative phase of the excitation frequency ω , so the digital angle φ can be obtained by taking the difference between these two PLLs digital output.

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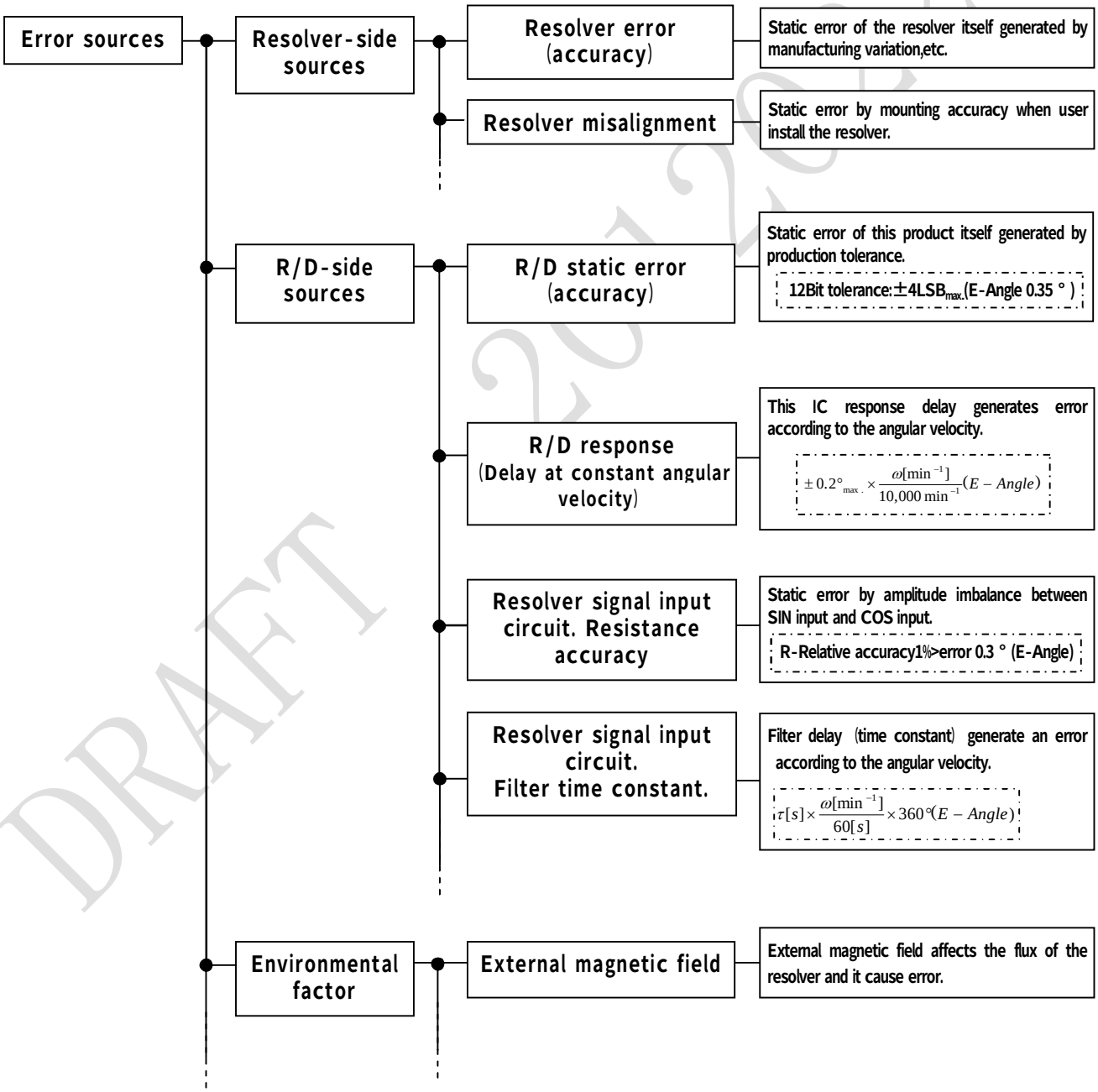
11.2 About the error of resolver system

Resolver system with this product causes an error against actual angular position by resolver accuracy, this smartcorder accuracy, peripheral configuration error, etc. In this chapter, explain the error sources of resolver system and general estimation method of total error.

11.2.1 Error sources

There are error souces of resolver system like the following.



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11.2.2 Error estimates

Total error of the resolver system using this IC is a combination of potential errors which include static error that typically come from resolver itself or this IC itself, and proportional error of angular velocity that come from delay of this IC or peripheral circuit depending on the angular velocity.

$$\varepsilon_{TTL} = \varepsilon_{ST} + \varepsilon_{DLY} + \cdots$$

While ε_{TTL} : Total Error of resolver system
ε_{ST} : Static error of resolver system
ε_{DLY} : Angular velocity proportional error

※ Each error might have different unit, and there are concepts which are "Number of multiple", "Mechanical angle", "Electorical angle". (Refer section 11.4 for each term). When estimating the error, please be careful to fitting the unit.

■Estimation of static error

Considering the estimation method of resolver system static errors which include resolver accuracy and error of this IC itself and the variation of the peripheral circuit or configuration, the easiest way is taking the sum of the maximum error caused by factors. But it is difficult to assume a probability that all of errors will be worst value, considering process capability, etc. Also it might need excessive precision characteristic to satisfy system, and then system cost might lead to increase.

Then static error of resolver system estimates normally with root mean square (RMS) method.

$$\varepsilon_{ST} = \sqrt{(\varepsilon_R)^2 + (\varepsilon_S)^2 + (\varepsilon_{RD})^2 + (\varepsilon_i)^2} \cdots$$

While ε_{ST} : Static error of resolver system
ε_R : Error of resolver
ε_S : Error of resolver misalignment
ε_{RD} : Static error of this IC itself
ε_i : Resolver signal input circuit :Resistance accuracy

■Estimation of angular velocity proportional error

Angular velocity proportional error of resolver system is caused by response delay of this IC and signal delay which depend on the filter circuit constructed in resolver input circuit. This error is getting bigger with higher angular velocity, and it is obtained by converting the angular displacement from total delay time at applied angular velocity. Then it is estimated as the sum of individual errors due to the delay factor.

$$\varepsilon_{DLY} = \varepsilon_{RDDLY} + \varepsilon_{FLTDLY} + \cdots$$

While ε_{DLY} : Angular velocity proportional error of resolver system
ε_{RDDLY} : Angle error of this IC response delay
ε_{FLTDLY} : Angle error of the filter time constant at resolver signal input circuit.

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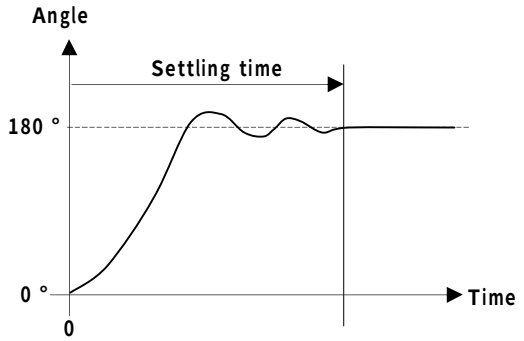
11.3 FAQ

■Questions on the performance･characteristic of R/D conversion

Q	How much time it takes to convert R/D ?
A	Assumed as delay time from input of resolver signal to output of its angle data. Then it will be 3.3μs max. Response spec is converted value from above time to the angular displacement while constant speed of rotation.

Q	Please tell us a frequency response of negative feedback loop which realize R/D conversion.
A	When the recommended value of spec is applied between LFLI-LFLO and LFUI-LFUO, bandwidth of this control system shows about 2.2kHz. A response that input angle change at higher frequency than 2.2kHz will have -40dB/dec characteristic.

Q	What happen to the output data in case of resolver signal input is above maximum angular velocity?
A	An absolute angle data can follow over spec velocity as long as the internal VCO output is not saturated, but a change in the data will not be only one LSB. Along with this A/B/Z output might generate missing pulses. When the rotation speed is getting faster and the internal VCO output is saturated, it will not be able to follow the rotation of resolver and output shows irrevant data (loss of synchronism condition).

Q	What is settling time ?
A	The time to respond when resolver signal input change as step-like 180 ° . This is one of the indicators which show control system performance of R/D converter. There is no chance to work this step(180 °) response for the actual resolver signals. 

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Q	In the operation of the rotating resolver, output angle data against actual resolver angle is shifted with the direction of rotation. Are there any considerable factor?
A	Typical factors are following. **(1) Displacement of the device which put on the resolver.** There might become angular displacement depending on direction, caused by mechanical misalignment of device like backlash of gear, etc. The problem of this factor is only depending on the rotation direction, and it is not depend on revolution speed of resolver. **(2) Time constant of filter circuit.** If resolver signal input to AU6803 (AU6804) through filters, there might show angular displacement depending on rotation direction while high speed resolver operation, caused by time constant delay value of filter circuit. The problem of this factor normally tends to be large in proportion to the number of revolution. **(3)AU6803 (AU6804) response (Delay time of response) :** Delay time from resolver signal input to corresponding angular data output might cause of the deviation angle which depend on the direction at high speed resolver operation. The problem of this factor normally tends to be large in proportion to the number of revolution.

Q	While we have connected the filter to the outside of LFUI, LFUO, LFLI, LFLO pins, Why do we need these parts? For what?
A	It is configured the compensator for stabilization and improvement of the characteristics of negative feedback control system. If not, the negative feedback control system will be collapsed and it can not operate R/D conversion successful.

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■Questions about the resolver interface.

Q	Is it possible to use R/D converter without using the output signal terminal R1/R2 ?
A	Can not be used. Resolver signal obtained by performing a resolver excitation of external oscillator or something can not make R/D conversion in principle. So it does not be subject for R/D conversion.

Q	A direct excitation function of the AU6803 (AU6804) output can not generate voltage of the resolver specification.
A	Direct excitation voltage is the product of resolver input impedance (below 200Ω) and excitation output current. If you need a larger excitation voltage, you need to excitation via the external booster amplifier which source is AU6803 (AU6804) exciting output. It will be judged by considering noise effect whether we need to excitation resolver with the larger voltage or not. And it will not be always required such larger voltage amplitude.

Q	How does this affect you connect a load of more than 200Ω between R1-R2?
A	There will be assumed that enough current can not flow in, the excitation signal is saturated, can not get normal waveform. In addition, signal amplitude will be smaller than the calculated value due to saturated signal.

Q	If e make short between R1-R2, IC will be broken ?
A	There is no damage by overcurrent, etc because output is current control type.

Q	What kind of behavior if you do not enter anything resolver signal ?
A	It will be the situation that control loop is broken. Then the angles of the output data repeatedly UP/DOWN or runaway, so it will be undefined behavior.

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Q	**Please tell the voltage specification of S1~S4 input signals.**
A	**Input signal voltage range of each terminals must be 0~VCC as absolute maximum rating. A operation acceptable range will be about 1.1V~3.8V (reference value) and normally it works around 2.25V.** **For the signal level adjustment of operational setting, instead of adjusting terminal S1~S4, please adjust SINMNT/COSMNT voltage level which is 2Vp-p(typ) with COM potential center.**

Q	**As a noise countermeasure, would like to add normal-mode-capacitor C_N .** **How much capacitor value do you recommend?**
A	**C_N insertion is required as counter action for some negative effect of electorical noise injection. Actual cap value can not specify due to it depend on the noise level.** **Too large cap value might cause larger attenuation and phase change of resolver signals. So C_N value variability might cause an imbarance between SIN and COS, and it becomes error factor. Be careful about it.**

Q	**In case of monitor output exceed 3.5Vp-p, what kind of adverse effects can we expect?**
A	**It is assumed like voltage saturation and abnormal waveform for monitor output.** **These will be error factors for R/D conversion.**

Q	**Would like to monitor analog velocity output by analog port of microcontroller.** **But there is a big offset exist and can not be used it.**
A	**Analog velocity output shows large variation and bigger influence of the temperature. So it might use to check only standard level.** **Then please understand that we can not recommend using this signal for speed control, etc.**

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■Questions about the default setting function.

Q	Trying to set the default setting terminals for pull-up side. The default setting terminals have internal pull-up resistor. Still do we need to add external 10kΩ pull-up resistor for setting pull-up side?
A	In functiobnal view point, the terminal will be pull-up setting without external 10kΩ pull-up resistor. But internal pull-up resistor value of IC is large one so in terms of noise immunity it is weak. Then we recommend to add external 10kΩ pull-up resistor.

Q	There is an excitation mode selection in default setting function. What is difference between current excitation mode and voltage excitation mode?
A	An excitation mode setting function sets the allowable range of the internal phase shift according to the phase shift value caused by the situation of the peripheral circuits. This IC's acceptable range of the phase shift between an excitation waveform component of R1-R2 current output and an excitation waveform component of the output voltage monitor is as follows. ■Current excitation mode ： +90° ±45° ■Voltage excitation mode ： 0° ±45° A main impedance of resolver will be L component and depending on excitaion type there will be different phase value between an excitation waveform component of R1-R2 current output (source of excitation signal) and an excitation voltage phase. That is why we provided this function. Since this is a function to change the internal setting, excitation output between R1-R2 is not changed by this setting difference.

Q	Are there any effects when we used a situation which exceeds the allowable range for each phase shift in the excitation mode setting?
A	There might be 180° inverted data despite the fact that there is normal resolver configuration.

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■Questions about the serial input setting function.

Q	While setting the serial, what happen in the situations which send only (ex) 8 bits data and SSCS set to "H" ?
A	This is a shift register so newly input data update "Bit12" value and existing data are shifted to neighbor register which have smaller number. Let's assume that when you enter up to 8 Bits. Input data (First Bit to last 8th Bit) enterd serial setting register Bit5 to Bit12. And remaining set of Bit1~4 contents was 8 bit shifted from previous Bit9~12 contents. <Serial configuration register contents before updating>

Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12
Data A	Data B	Data C	Data D	Data E	Data F	Data G	Data H	Data I	Data J	Data K	Data L

<Contents of register after setting 8 Bits serial data>

Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12
Data I	Data J	Data K	Data L	Data M	Data N	Data O	Data P	Data Q	Data R	Data S	Data T

Before Bit9～12 data

8Bits serial input data

Q	While setting the serial, what happen in the situations which send longer bits (ex: 16 bits) data and SSCS set to "H" ?
A	This is a shift register so last 12 input data was set in 12 shift register. Other data before last 12bit data is discarded. Let's assume that when you enter up to 16 Bits. The contents of 5Bit ~ 16Bit input data can be set in serial setting 12 bit register.

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■Questions about the output interface.

Q	In the situation of digital output terminals might be shorted each other , short to VDD or GND, what kind of issues will be appear when the power is active?
A	When the voltage is different between the shorted pin (One side “H” and the other side “L”), excessive current flow from “H” to “L”, heating up, and finally IC might be damaged.

Q	Would like to get 8bit parallel output data. How can I do?
A	AU6803（AU6804） have only 12bit-mode setting. If you ignore the lower 4 bits, remaining data looks like 8 bits.

Q	There might be 1LSB difference between parallel data and serial data even if they captured at the same timing. Why does it happen?
A	It caused by the different latch timing to get data internally. Update timing of the serial output data is half cycle of the update for the parallel output data. Then there might be 1LSB difference even if captured at the same time according to the relationship of data capture cycle and data update timing.

Q	Is A/B/Z output from the parallel data pin (Pulse equivalent to encorder mode) the same as A/B/Z output of independent terminal? Is it possible to be used at the same time also?
A	It is the same output. And it is also possible to use at same time.

Q	Using encorder equivalent pulse mode, A/B pulse duty looks unstable while resolver rotate with same speed. What is possible cause?
A	Encorder equivalent pulse output of this IC is theoretically poorer performance than optical encorder pulse output. Due to the affect of resolver potential error and R/D potential error and also R/D conversion principle itself, it is possible to be disordered pulse duty even if in normal operation condition.

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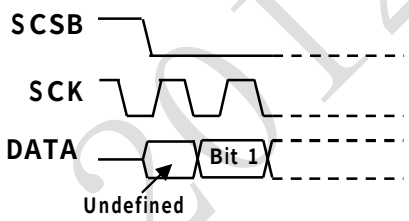
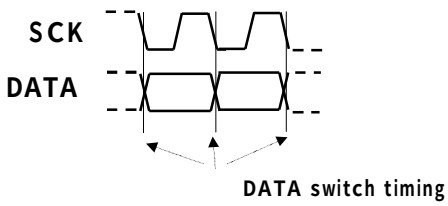
Q	For the digital output, serial interface output and parallel interface output and also independent terminal A/B/Z output are prepared. Do we need to use all output?
A	On the behavior of this product it is not a problem even if it uses the output of either. According to the system environment, please use appropriate interface or output.

Q	In serial output case, after SCSB falling edge, is the data which is before first SCK falling edge unnecessary?
A	No need. After SCSB falling edge, output data which shows until SCK falling edge is undefined value. Please ignore it. 

Q	To read the serial output data with above system, which is better trigger? SCK rising edge or SCK falling edge?
A	Please use SCK rising edge. Serial output data change with SCK falling edge timing. Then if you read the data with SCK falling edge, there might read false data depending on read timing. 

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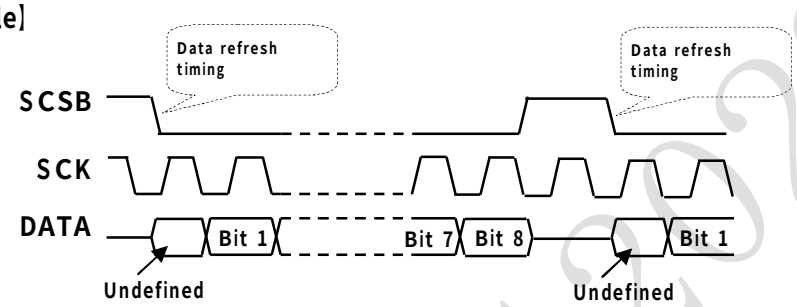
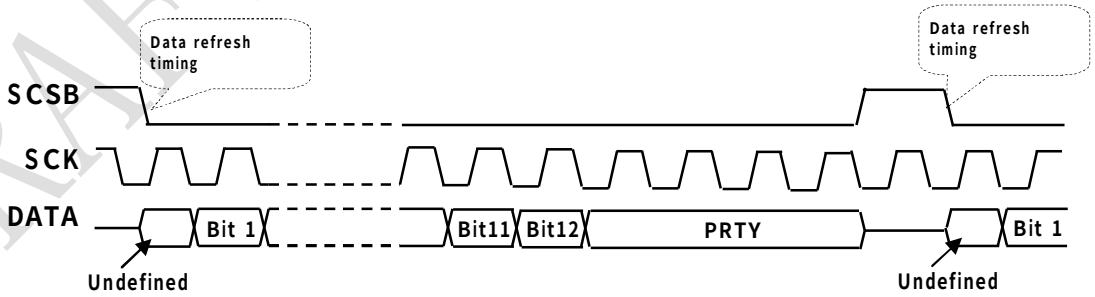
Q	Plan to use serial output function with absolute output mode. But data need only 8bit due to above system configuration. How should I handle about serial output data?
A	Please exit serial output sequence (SCSB=L⇒H) after 8th serial data output. ※ Even in the middle to end, data is refreshed and next output mode start with MSB data. [Example] 

Q	Plan to use serial output function with absolute output mode. But data need 16bit due to above system configuration. How should I handle about serial output data?
A	After continuing to output up to 16 serial clock with keeping "SCSB=L" , please exit serial output sequence. After PRTY has been output, keeping "SCSB=L" and SCK can continue to enter. Then output data will keep PRTY data. 

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■Questions about the exciting clock.

Q	When this product operates in external clock mode, is it possible to connect crystal oscillator or ceramic resonator directly as external clock input?
A	Can not be connected. It must be only digital clock signal generated by crystal oscillator, etc.

Q	In external clock mode, clock frequency specification shows 10MHz±20%. When a clock which exceed its frequency range applied, what kind of problem does it happen?
A	The considerable issues are decreasing of maximum tracking rate, occurrence of missing encoder pulses, and the data might not be settled. It is also possible that the current value of excitation output does not satisfy the specification values.

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■Questions about the power sources.

Q	What kind of problem does it expect if you do not used in the same potential VCC, VRR, and VDD ?
A	It may cause abnormal heat generation or failure. Each power supply is connected through a diode. When the potential applied to diode is getting bigger than the diode forward voltage, excessive current will generate.

Q	When the power is turned on, what problem are you having not been turned on at the same time VCC, VRR, and VDD.
A	There is possibility not to make default setting correctly. The power-on reset has been granted to the VCC pin. While pull-up/pull-down of default setting terminal usually connect to VDD potential. If VCC is applied but VDD is not applied, in this case there might be miss-setting in default setting sequence and incorrect data might be read. Also each power supply is connected through a diode. When the potential applied to diode is getting bigger than the diode forward voltage, excessive current will generate and it might cause potential problem.

Q	I would like to excite resolver with external voltage booster amplifier which signal source is exciting output of AU6803(AU6804). Is there any timing constraint for the exciting amplifier power up?
A	There is no special restriction. If the power supply of exciting amplifier turns on after the device power supply, the device will not be able to get resolver input signal. Then it might cause fault detection with the balance of the mask error period.

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■Questions about the function of fault detection.

Q	Does the fault detection result affect the behavior of R/D conversion?
A	Does not affect. The fault detection function is independent to R/D conversion so fault detection result does not give a constraint on the output of R/D conversion. It will continue to operate R/D conversion as abnormal condition. But when it return to the normal state from abnormal resolver signal state or breaking of resolver signal line, once this system reset the R/D conversion loop (PLL).

Q	When the error reset at ERRSTB, How long time do we need to set reset situation (ERRSTB=L) ?
A	Minimum 40ns (Same as maximum time to be extended ERRHLD signal)

Q	Does the error reset function by ERRSTB affect the behavior of R/D conversion?
A	Does not affect. ERRSTB is a function to reset ERRHLD and ERRCD1～3 outputs only.

Q	DC bias resistance was connected in reverse polarity. Nevertheless error detection looks work at signal desiconnection situation. Why is the error detected?
A	Depending on the angle there might be detected failure by abnormal resolver signal. And due to connect in reverse polarity, in disconnection case, monitor output voltage expect shift to GND-side. Then correct R/D conversion can not operate and it is considered that abnormality have been detected by abnormal R/D conversion.

Q	During 70ms (max.) error mask period after VCC up, what is ERR/ERRHLD output behavior?
A	L output will be forced regardless of abnormality detection in this product.

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■Questions about the function of Built-In Self-Test(BIST).

Q	If want to run consecutively to excute self-test (BIST), Does error resetting activity need to run in every BIST operation?
A	Error reset can be performed only once after running the last self-test(BIST) operation. ERRHLD "H" output during the excution of the BIST will be remained even if it returns to normal operation after BIST. Then error reset operation is required.

Q	After BIST operation, please tell the conditions when BIST result show "abnormal BIST (BIST code "1111")".
A	There are two cases explained below. ■The case that the BIST result is NG at the time of serial output. ■The case that you run BIST sequence with a reserved BIST setting code of serial input setting register.

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■Questions about the applications.

Q	Is it possible to use with phase modulation type (BRT) resolver?
A	No. This product only supports amplitude modulation type (BRX) resolver.

Q	Is it possible to use multiple AU6802N1 which connect same one resolver?
A	Can not be used. Resolver signal obtained by performing a resolver excitation created by an external oscillator (example) can not operate R/D conversion normally due to principle issue. Then this case will not be eligible for R/D conversion.

Q	How much cable length between resolver and AU6803(AU6804) can we extend?
A	It can not to say simple because it depend on the type of cable and wiring, but basically there are not much problem about cable length itself which is a few meters except for noise superimposed case, etc.

Q	Is it possible to connect the measuring instrument to confirm the signal of LFUO or LFLO ?
A	Connecting the measuring instrument itself can be possible due to there are protective resistance exist. But there is the possibility of deterioration in precision of the output angle by adding an additional load. So we do not recommend.

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11.4 Terms and Definitions

Term	Number of multiple (N)
Definition	Show 1/2 the number of poles (pole pair) . Display is added with "X".

Term	Mechanical angle (θ m)
Definition	Rotational angle of resolver rotor (Mechine axis)

Term	Electorical angle(θ e)
Definition	Machine 1 cycle 360 ° / N (number of multiple) define as electorical 1 cycle 360 ° . θ e＝N θ m

Term	Resolver input impedance (Zro)
Definition	Resolver exciting-side impedance

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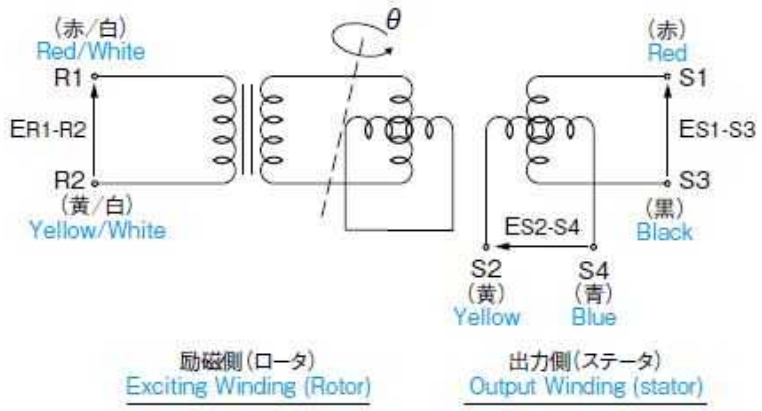
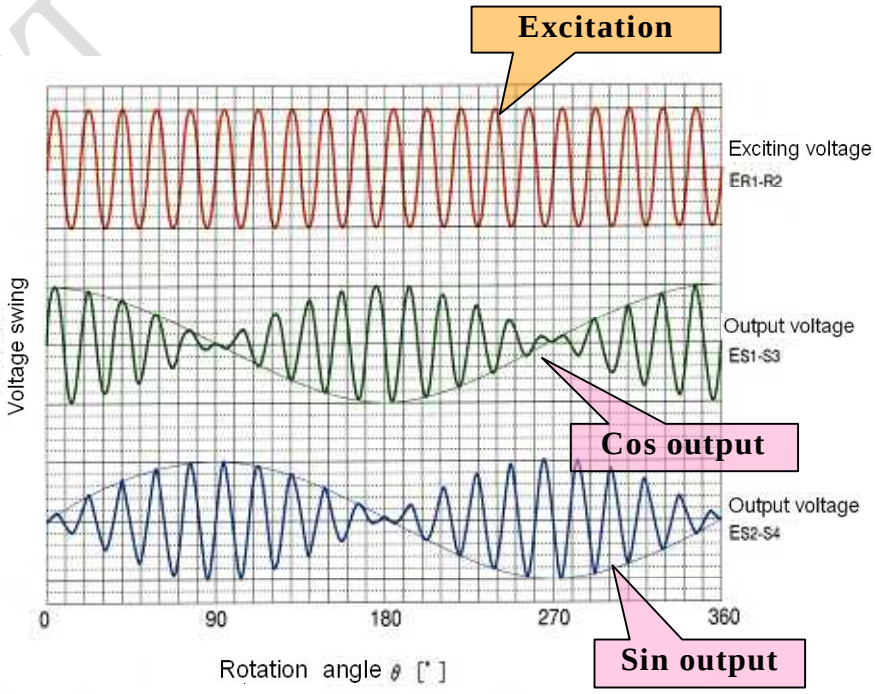
Term	BRX
Definition	1Phases-in/2Phases-out (Amplitude moduration type) brushless resolver. ■Configuration of resolver  ■Output voltage equation Excitation : $E_{R1-R2} = E_1 \sin\omega t$ Output : $E_{S1-S3} = kE_1 \cos\theta \sin\omega t$ $E_{S2-S4} = kE_1 \sin\theta \sin\omega t$ ■Exciting signal and resolver signal waveform 

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12. Revision history

Revised date	Revision	Location of revisions	Revision content·reason
2012.2.29	Draft version	—	—

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